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FINAL REPORT

VOLUME II-DIGITAL VCO TECHNIQUE

ONE WAY DOPPLER EXTRACTOR

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by

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ABSTRACT

Volume II of this report presents a feasibility analysis and trade-offs for a One Way Doppler Extractor using digital VCO techniques. The method of doppler measurement involves the use of a digital phase lock loop. Once this loop is locked to the incoming signal, the precise frequency and hence the doppler component can be determined directly from the contents of the digital control register. Since the register size determines the system's quantization error, it can be made arbitrarily small by carrying a sufficient number of bits. Other errors are due to the signal-to-noise ratio and the reference oscillator stability. The only serious error source is due to internally generated noise. Techniques are presented for minimizing this error source and achieving an accuracy of 0.01 Hz in a one second averaging period.

A number of digitally controlled oscillators are analyzed from a performance and complexity point of view. The most promising technique uses an arithmetic synthesizer as a digital waveform generator. RCA is currently designing an LSI array as part of an arithmetic synthesizer development using CMOS/SOS technology for minimum power dissipation at clock rates up to 20 MHz. A configuration of a One Way Doppler Extractor making use of this development is recommended for future exploitation.

FOREWORD

This is a final report for NASA Contract NAS 9-13517 covering the period from 1 July 1973 to 1 November 1974. The program consisted of the following three phases:

- 1. Feasibility study and trade-off analysis
- 2. Breadboard development
- 3. Feasibility study of digital VCO techniques

The overall program was conducted under the direction of Edward Nossen. Both feasibility studies were carried out by Eugene Starner. The breadboard development was directed by Seymour Klein; major contributors to the breadboard development were Richard Blasco, Daniel Hampel and John Yanosov. The preliminary design of flight hardware was also headed up by Seymour Klein.

Volume 1 of this report contains 3 parts:

Part 1 - The feasibility study and trade-off analysis

Part 2 - Breadboard development

Part 3 - Flight hardware design

Volume 2 of this report covers the feasibility study of digital VCO techniques. Dr. Stephen Goldman's assistance in the preparation of that volume is greatly appreciated.

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SECTION 1

INTRODUCTION AND SUMMARY

Volume 1 has described the vernier technique of doppler extraction and the test results obtained from the breadboard equipment. While the vernier technique has demonstrated a great improvement in doppler resolution compared to previous techniques, there are some constraints. For example, the delay time between a count command and its execution is dependent on the desired resolution and the doppler frequency. In applications where delay time is of little importance, the vernier technique can provide a resolution which is comparable to the limitations imposed by the best oscillator. However, when a rapid response is sought the resolution may have to be degraded intentionally.

RCA has continued to search for techniques for doppler extraction which can provide arbitrarily small doppler resolution at practically zero delay times. Furthermore, these techniques must be relatively inexpensive to implement for wide spread application, and must be packagable in a small volume and consume little power for space or portable environments.

The digital technology has advanced at a rapid pace in recent years. Both ends of the spectrum have progressed. Counting circuits operating at speeds of 500 MHz are readily available, but at the expense of power dissipation. It is thus possible to achieve excellent doppler resolution and speed of response by employing high speed clocks and counters to measure the period of doppler cycles. The complexity, power dissipation and cost of using such high speed circuits does not make this an attractive solution. On the other hand, with the advent of relatively inexpensive Large Scale Integration (LSI) digital technology, it is now possible to perform many frequency synthesis and measurement functions in a more digital fashion. Use of thousands of gates or hundreds of flip-flops is no longer a deterrent to digital implementations, since this may now represent one or a few LSI arrays, which are designed and produced by automated techniques. The power consumption of these LSI chips is also very

small, particularly when CMOS technology is used.

This volume reports on various digitally controlled oscillator techniques and their application to the precision measurement of doppler frequencies. The basic concept employs such a digitally controlled oscillator in a phase locked loop, which acquires, tracks and measures the doppler frequency. The nominal value of the incoming frequency is represented by a digital number, which in turn controls the reference frequency synthesizer. At phase lock the incoming frequency and the generated frequency are identical, since only a small phase error will exist. The precision of the frequency measurement is unlimited, since it merely requires a few more bits in the control registers to split one cycle of doppler to an ever smaller fraction, For example, a 20 bit register could provide a resolution of one millionth of a doppler cycle.

The accuracy of the doppler measurement depends on the usual external parameters. In a one way doppler measurement, the accuracy and stability of the frequency standard is the most serious limitation. In two way doppler systems with a common transmit and receive oscillator, this is a much less serious problem. The signal-to-noise ratio at the receiver output also affects the doppler accuracy. In general, when the receiver is used for voice or data communication, the received power is more than adequate to obtain a high signal-to-noise ratio on the doppler shifted carrier component. Residual carrier systems provide this carrier component directly, while the newer suppressed carrier modulation techniques provide strong reconstructed carrier components to allow error free data demodulation. A carrier signalto-noise ratio of 24 dB or better is sufficient to achieve a 0.01 Hz doppler accuracy in a one second period. The signal-to-noise ratio can be controlled by making the loop bandwidth relatively narrow, although a 335 Hz minimum bandwidth is required to track the doppler rate with minimum error. The loop acquisition time is also influenced by the loop bandwidth. But again the acquisition time is sufficiently short for the bandwidth dictated by the doppler rate tracking requirement.

With all these performance advantages and the potential for low cost LSI implementation there must be a disadvantage. The only problem in the arithmetic synthesizer type of digitally controlled oscillator is internally generated noise due to sampling and quantization of the digital waveform generation process. While the digital logic can easily use 20 or even 30 bits, the practical limit of low cost digitalto-analog converters is 10 to 12 bits at the present time. A 16 bit D/A converter is available but it is large and slow, and therefore. only suitable for the generation of lower frequency waveforms. 10 bit D/A converter produces a noise floor of 60 dB, which is perfectly adequate for doppler extraction. However, if the synthesized waveform is to be multiplied by a factor of about 100 to interface at 76 MHz, the noise will be increased by 40 dB. The internal noise will now limit the doppler measurement accuracy. Other noise sources in the frequency synthesis process, such as spurious frequencies, behave in a similar fashion. Several techniques for the reduction of spurious frequencies are presented, and further work in this area is recommended as part of future efforts. To minimize the effect of internally generated noise, it is most desirable to use the digital synthesizer at output frequencies of about one megahertz or less, instead of multiplying its output. Consequently the incoming doppler signal on a 76 MHz or 19 MHz bias frequency should be translated by means of a stable, fixed oscillator to about 1 MHz or For the USB transponder the 76.083 MHz interface signal can be translated to 1.083 MHz by means of a stable 75 MHz oscillator, as currently used in the vernier breadboard. The digitally controlled phase lock loop can then extract doppler with a 0.01 Hz accuracy in a one second averaging period.

RCA is currently developing an LSI version of an arithmetic synthesizer under an Air Force contract. The arithmetic synthesizer or digital waveform generator has been found to be the most promising solution for LSI integration and hence low production cost for digital frequency synthesizers. The digital waveform generator is covered by an RCA patent (#3689914) which is reproduced in Appendix A. In the LSI version of this synthesizer all digital functions will be integrated on a single array using silicon gate, double epitaxial CMOS/SOS technology. The design will allow operation at clock rates

up to 20 MHz at very low power consumption. The basic digital array will contain a stackable 8 stage synthesizer. Three LSI chips can thus provide a 24 bit synthesizer to satisfy the doppler extractor requirements.

It is recommended that a doppler extractor breadboard using the digital waveform generation techniques be built to verify the analytical performance predictions. From this breadboard accurate flight hardware projections can then also be made.

SECTION 2

DIGITAL VCO DOPPLER EXTRACTOR

2.1 GENERAL TECHNIQUE DESCRIPTION

A digital VCO (DVCO) is a frequency synthesizing device whose output frequency is precisely specified by a digital number programmed into a frequency register. By changing the number in the register the output frequency is changed proportionately. There are several methods of implementing a DVCO, but in general, all of the techniques convert a stable known reference frequency (clock frequency) to the desired output frequency by arithmetic operations on the digital frequency register number and/or the clock frequency. Figure 2-1 shows a functional diagram of a typical digitally controlled oscillator. Since there are no bandwidth limiting devices in the DVCO, the output frequency is changed almost immediately after the register number is changed.

To extract doppler information from a doppler reference signal, the digital VCO can be phase locked to the doppler reference in such a way that the feedback error signal controls the frequency register number and maintains phase lock. This is shown in the block diagram of Figure 2-2. The phase detector output error signal is low pass filtered and fed to an analog to digital converter (A/D). The numerical output of the A/D converter is used to change the frequency register so that the DVCO output frequency remains in phase lock to the doppler reference signal. At phase lock, the DVCO frequency and the doppler reference frequency are equal. Thus, the digital number in the frequency register is proportional (or functionally related) to the doppler reference signal. By monitoring the register number the doppler reference frequency, and hence the doppler frequency, can be determined. By continuous monitoring of the register number the time history of the doppler frequency can be determined.

The rate at which the frequency register is updated is governed by the bandwidth of the low pass loop filter. Wide bandwidths allow rapid updates and low phase error between the register number and the doppler reference frequency. However, they also admit more noise.

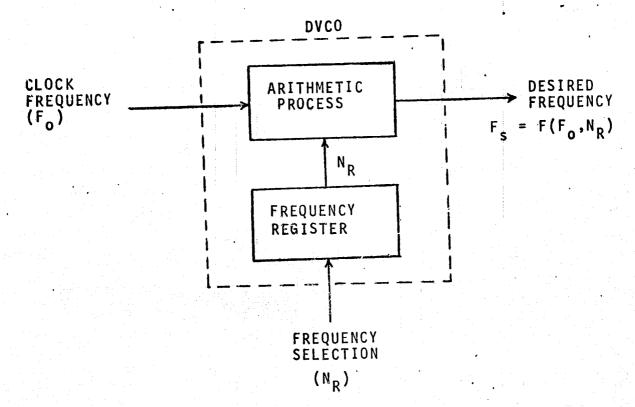
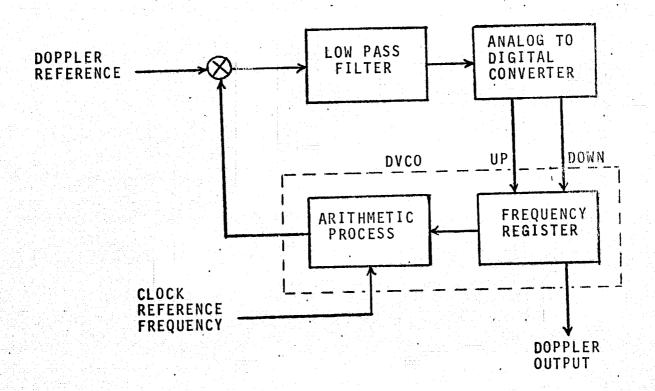


Figure 2-1. Digitally Controlled Oscillator



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Figure 2-2. Digital VCO Used as a Doppler Extractor

Acquisition of the doppler reference by the DVCO can be accomplished simply by presetting the desired number in the frequency register. If the doppler reference is known to within the loop bandwidth, acquisition should occur almost immediately. A sweep acquisition can be implemented by periodically increasing (or decreasing) the register number by a constant increment. The DVCO frequency will then be stepped in precise frequency increments. When acquisition occurs the register incrementing device can be removed.

2.2 S-BAND TRANSPONDER INTERFACE TECHNIQUES

*

In order to extract the doppler information from an S-band transponder, the digital VCO can be phase locked to any suitable doppler reference signal in the transponder. With the present transponder designs, a doppler reference signal exists at either the transponder VCO output (\implies 19 MHz) or a times 4 VCO output (\implies 76 MHz). If the speed of the arithmetic logic in the DVCO allows generation of frequencies as high as those listed above, the DVCO can be directly phase locked to either the 19 MHz or 76 MHz interface. However, in several DVCO implementations the output frequency is limited to a few megahertz, primarily caused by the speed of the arithmetic processor logic. With these DVCO implementations, the DVCO frequency can be multiplied to the transponder interface frequency with the use of a multiplying phase locked oscillator. This multiplied frequency is then phase locked to the transponder interface. A block diagram of this technique is shown in Figure 2-3.

Alternatively, the DVCO frequency could be translated to the transponder interface frequency by mixing the DVCO frequency with a fixed clock derived frequency. A block diagram of this technique is shown in Figure 2-4. This technique has the advantage of retaining a higher percentage of the S-band doppler shift on the frequency register output and also does not multiply the phase noise on the DVCO output.

A third possible interface between the DVCO and the S-band transponder is to use the DVCO as a local oscillator for the transponder. A block diagram of the technique is shown in Figure 2-5. In this configuration the DVCO supplies all mixer injection

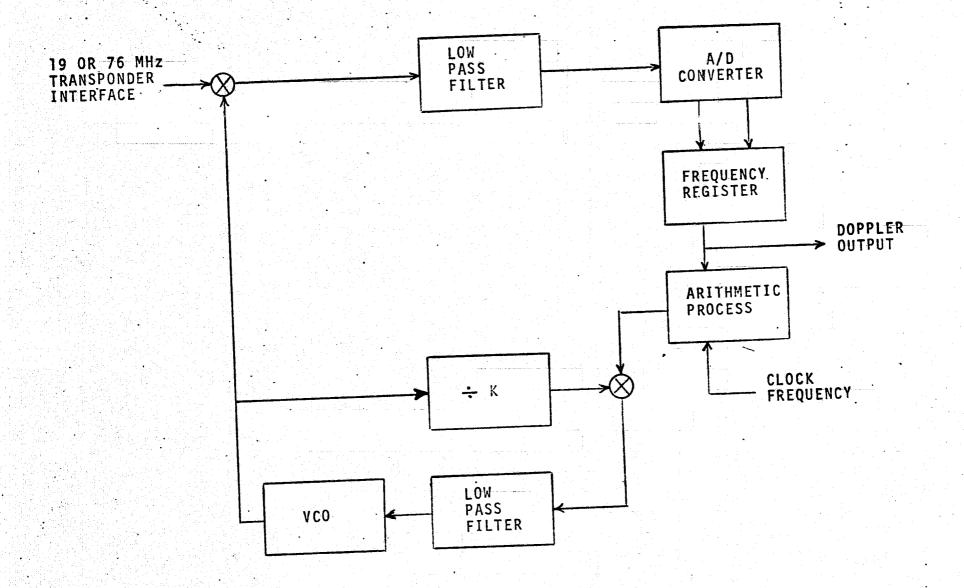


Figure 2-3. Multiplication of DVCO Frequency to Transponder Interface Frequency

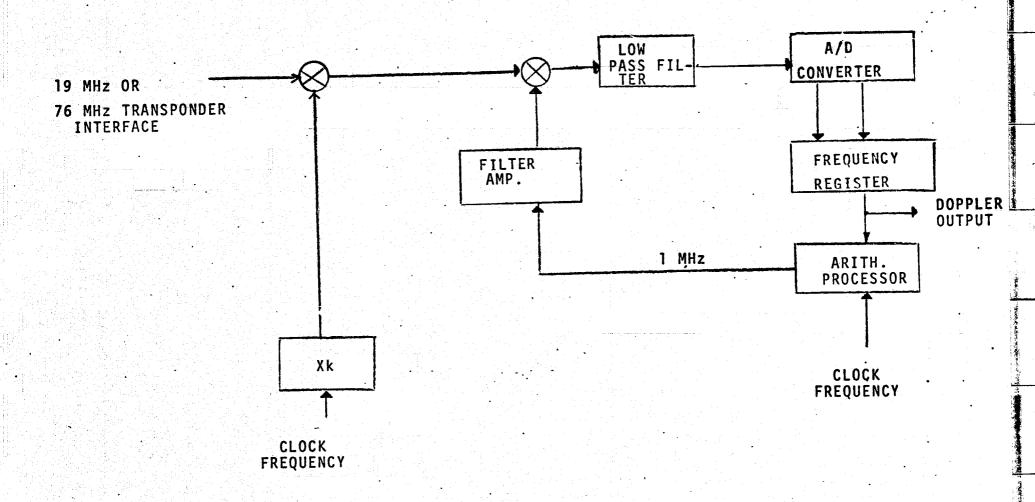


FIGURE 2-4 TRANSLATION OF TRANSPONDER INTERFACE FREQUENCY TO DVCO FREQUENCY

FIGURE 2-5 DVCO USED AS TRANSPONDER LOCAL OSCILLATOR

frequencies and obtains phase lock to the S-band frequency by means of the last mixer stage. This technique has the advantage of supplying a multi-frequency transponder capability combined with doppler extraction.

2.3 GENERAL SYSTEM REQUIREMENTS

Regardless of the type of digital VCO used for doppler extraction, some of the system parameters can be defined for all of the techniques. These include loop bandwidths, signal to noise levels, and doppler resolution (quantization level) of the digital VCO.

It is desired to measure the doppler off-set to an accuracy of approximately 0.2 cycles (0.1 Hz in a 0.5 second averaging time) referenced to the S-band doppler shift. However, since a very high degree of precision is attained by the digital VCO, a design goal of 0.01 cycles (0.01 Hz in | second of averaging) for each error source has been established as a baseline for system selection and trade-offs. With this level of precision some of the system parameters can be defined as described in the following paragraphs.

2.3.1 DVCO TRACKING LOOP BANDWIDTH

In order for the digital VCO to maintain an accurate phase lock to the S-band interface frequency, the DVCO loop bandwidth should be made very wide. When a doppler rate is present the tracking error increases and worst case tracking error occurs at the greatest doppler rate. From the Statement of Work the maximum doppler rate could be as high as ± 4500 Hz/second (range rate acceleration of ± 610 meters/sec² at 2200 MHz S-band frequency). For a given loop bandwidth the tracking error is given in reference (9) as:

$$\theta_{a} = \frac{\dot{f}_{d}}{\omega_{n}^{2}} \approx \frac{\dot{f}_{d}}{4 \beta_{L}^{2}}$$

$$B_{1} = \sqrt{\dot{f}_{d}/4 \theta_{a}}$$

 $m{\Theta}_{a}$ is the tracking error in cycles where 1 cycle equals $2\, \mathcal{T}$ radians.

F_d is the maximum doppler rate

 $\omega_{\mathbf{n}}$ is the loop natural frequency

B, is the loop bandwidth

 \mathcal{Z}_{j}

With $\Theta_a \leq 0.01$ cycles and $F_d = 4500$ Hz/sec then $B_L \cong 335$ Hz. This loop bandwidth is required regardless of the technique used to phase lock the DVCO to the transponder interface frequency. For example, if the interface frequency is 19 MHz then the maximum doppler rate is divided by approximately 100. However, the DVCO must track this signal to an accuracy 100 times better, so that the tracking error referenced to S-band doppler is no greater than 0.01 cycles. Therefore $F_d/4$ Θ_a is a constant and the overall loop bandwidth of the DVCO phase locked loop must be $\Theta_a = 335$ Hz. This is the same as when the full doppler rate is being tracked.

2.3.2 DVCO ACQUISITION LOOP BANDWIDTH

If it is desired to have the digital VCO acquire the doppler shifted S-band interface frequency then the loop acquisition bandwidth must be sufficiently wide to allow the DVCO to pull in within a reasonably short time (a few seconds or less). From equation (4-31) of reference (9) the time to acquire is given approximately by

$$T_{p} = \frac{\left(\frac{\Delta\omega}{K}\right)^{2}}{2 \, S \, \omega_{n}^{3}} = \frac{\left(\frac{2 \pi \Delta F}{K}\right)^{2}}{2 \times 1 \times \left(2 \, B_{L}\right)^{3}} = \frac{4.93 \left(\frac{\Delta F}{K}\right)^{2}}{B_{L}^{3}}$$

where T_n is the pull-in or acquisition time

 ΔF is the maximum frequency off-set (2 Fd max.) referenced to S-band = $\Delta \omega / 2\pi$

B, is the loop acquisition bandwidth

K is the doppler division ratio at the transponder interface frequency.

is the loop damping coefficient = 0.5
 is the loop natural frequency

The above formula is only valid if (from equations (4-30) and (4-4a) of Reference 9):

$$\Delta \omega < 2 \sqrt{S w_n K_v} = 2 \sqrt{0.5 \times 2B_L \times \frac{2\pi \Delta F}{\theta_v}}$$

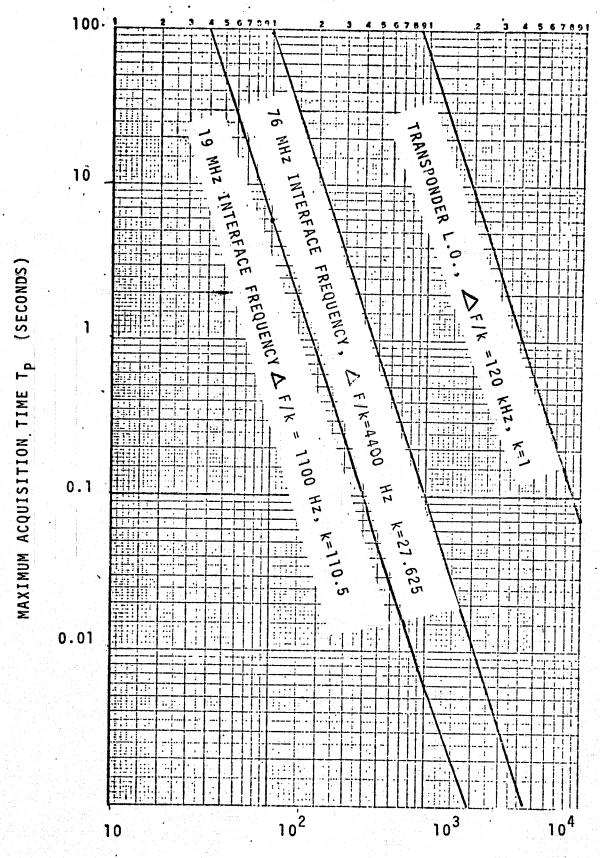
$$\therefore \Delta F < \frac{B_L}{\pi^2 \theta_v}$$

where Θ_V is the desired tracking error (0.01 cycles at S-band where 1 cycle = 2π radians).

Figure 2-6 shows the maximum time to acquire as a function of loop bandwidth and for the optional transponder interface frequencies. Two criteria are considered when selecting the loop bandwidth B_L : (1) the acquisition time and (2) the tracking error. With a 19 MHz interface frequency, the bandwidth required for less than 1 second of acquisition time is 180 Hz. However, 335 Hz is required for the maximum tracking error not to exceed 0.01 cycles. For the 76 MHz interface and the transponder local oscillator, the B_L required for a maximum tracking error of 0.01 cycles is 335 Hz. Since this is less than the bandwidth B_L required to acquire in 1 second, the 1 second acquisition bandwidths of 460 Hz (for the 76 MHz interface) and 4.2 kHz (for transponder L.O.) determine the minimum B_L .

If faster acquisition times were desired, the DVCO acquisition could be aided by means of a frequency sweeping circuit. An alternate technique would be to pre-set the DVCO to a frequency closer to the true S-band frequency. Since the frequency is specified exactly by the digital number this is easily accomplished, provided the instantaneous S-band frequency is known accurately enough.

Figure 2-7 shows the required accuracy to which the S-band frequency must be known in order to acquire within one second. The data are shown as a function of the loop bandwidth and the type of transponder interface. With the DVCO used as the transponder



DVCO LOOP BANDWIDTH B IN HERTZ

FIGURE 2.6 DIGITAL VCO ACQUISITION TIME 2-10

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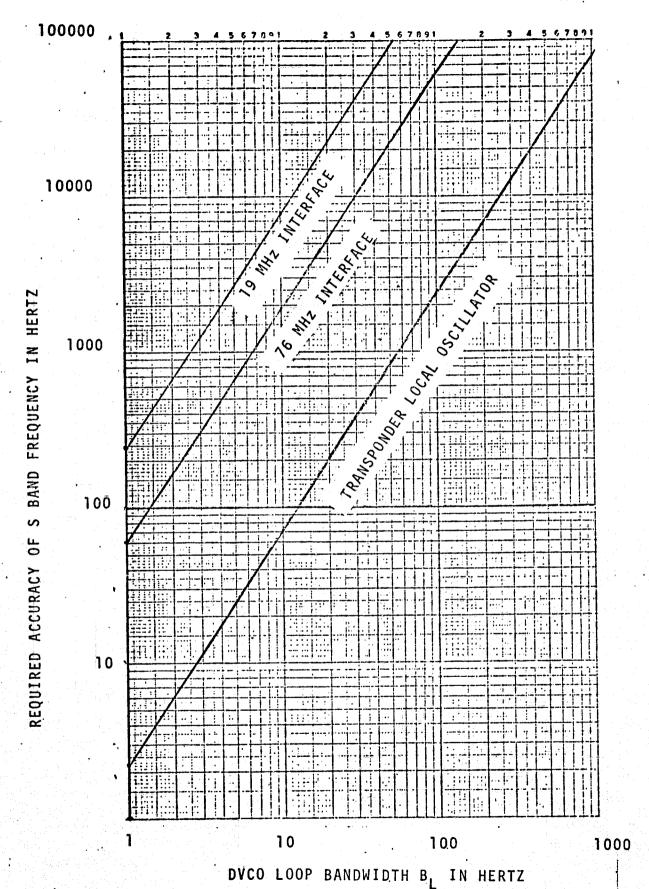


FIGURE 2.7 PRE-SETTING ACCURACY FOR ONE SECOND ACQUISITION TIME.

local oscillator an acquisition bandwidth of 335 Hz can be used if the instantaneous S-band frequency is known to within 2.9 kHz. Lower bandwidths can be used but only if the S-band frequency is known to tighter tolerances than the above.

Bandwidths wider than the 335 Hz minimum tracking bandwidth are desirable both for better tracking error and faster acquisition. The 335 Hz bandwidth is a minimum required value for tracking to within

.01 cycles of the S-band frequency. However, the minimum bandwidth of 335 Hz does set a requirement to be used for the selection of the digital VCO technique, since only those techniques which can operate with bandwidths of 335 Hz or more are desirable.

2.3.3 LOOP S/N LEVELS

2

In addition to the dynamic tracking error caused by a doppler rate, an additional phase error (jitter) is caused by noise in the loop bandwidth. As derived in Reference (1) and (9) this phase jitter caused a frequency jitter given by

$$G_{J} = \frac{1}{2 \text{ TT T } \sqrt{(S/N)_{Loop}}}$$
 (Referenced to S-band)

where (J is the frequency jitter in Hertz

T is the doppler averaging time

and (S/N) Loop is the loop S/N level

In the nominal 800 Hz bandwidth of the S-band transponder the above equation results in a 24 dB S/N requirement if the frequency jitter is to be 0.01 Hz (.01 cycles in 1 second).

If the digital VCO is phase locked to the transponder VCO output the DVCO will track this jitter resulting in the above frequency errors on the doppler measurement. If the digital VCO contains additional noise this will add to the jitter causing a further increase in the doppler error. The S/N requirement for the DVCO output reference frequency will depend on the technique for phase locking the DVCO to the transponder interface frequency. The requirements for the DVCO S/N levels are discussed in a later section, for the three types of transponder interface.

SECTION 3

DIGITAL VCO SELECTION

3.1 TECHNIQUES TO OBTAIN A DIGITALLY CONTROLLED OSCILLATOR

Several techniques exist to generate an output frequency which is controlled by a digital number. One technique is a Programmable Divide by N Phase Locked Oscillator in which a divided value of the output frequency is compared against a divided value of a clock reference frequency. By programming the division ratios, many different output frequencies can be generated. Another technique is the Iterative Synthesizer which uses a combination of frequency division and mixing to obtain an output frequency proportional to a digital input number.

A third technique employs an Incremental Phase Modulator which generates a controlled frequency offset from a given reference frequency. The offset is controlled by a digital value stored in a register. A fourth technique employs an arithmetic synthesizer which directly constructs a sine wave signal by accumulation of the digital number. A description of each of these techniques and their requirements is included in the following paragraphs.

3.1.1 PROGRAMMABLE DIVIDE BY N PHASE LOCKED OSCILLATOR

Figure 3-1 presents a block diagram of a $\frac{\bullet}{\bullet}$ N PLO. The reference oscillator output frequency f_R is divided by R and compared to the VCXO output frequency f_S divided by N. The value of f_S is changed by changing N. When

$$\frac{f_s}{N} = \frac{f_R}{R}$$

the PLO phase locks with an output frequency of f_s . The smallest frequency steps (resolution) that f_s can take are

$$f_s = N \times \frac{f_R}{R}$$

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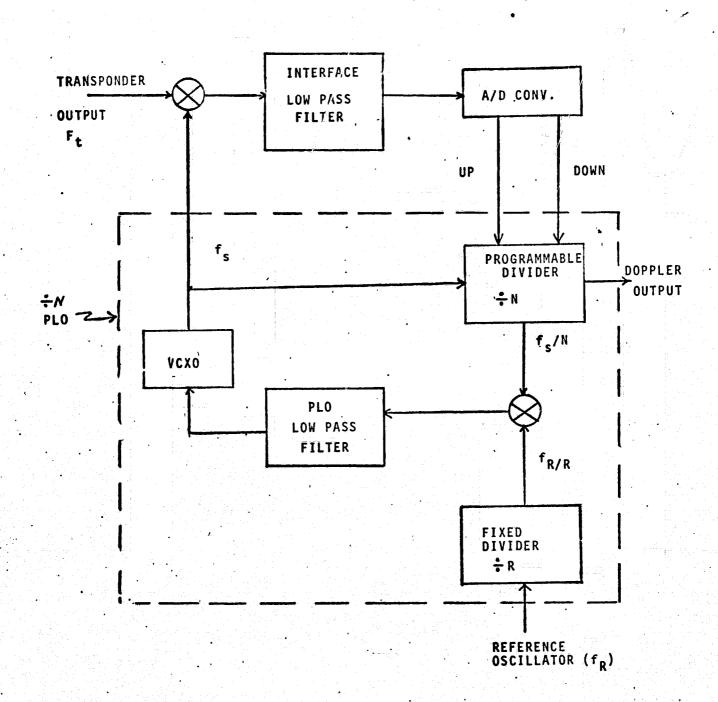


FIGURE 3-1 DIVIDE BY N PHASE LOCKED OSCILLATOR

ORIGINAL PAGE IS OF POOR QUALITY If the programmable divider PLO is locked to the 19 MHz transponder output directly, as shown in the figure, then a measure of the fractional doppler is obtained by monitoring the number stored in the programmable divider. Since:

19 MHz +
$$\frac{Fd}{110.5} = \frac{f_R}{R} = (N_0 + n) \frac{f_R}{R}$$

where Fd/110.5 is the doppler shift on the 19 MHz interface

No is the nominal value for N to produce a 19 MHz (zero doppler) comparison frequency

n is the change in N $_{\rm O}$ required to track the divided doppler shift.

Then:
$$F_d = 110.5 \text{ n } \left(\frac{f_R}{R}\right)$$

If Fd is to be resolved to .01 Hz, then a one unit change in n must result in a .01 Hz change in the computed doppler shift.

That is:

and
$$\frac{f_R}{R} \leq 10^{-4} \text{ Hertz}$$

The frequency ($f_{R/R}$) is the \div N PLO sampling rate. Thus, for a 0.01 Hz resolution the sampling frequency can be no larger than 10^{-4} Hz. Since suppression of incidental frequency modulation at the sampling frequency limits the PLO low pass filter to about one tenth the sampling frequency, the resulting overall loop bandwidth would be of the order of 10^{-5} Hz. This bandwidth is prohibitively narrow for implementation as well as for initial acquisition and tracking of doppler rates. Further, the VCXO would not remain locked to

fR/R due to VCXO phase noise frequency variations.

It might seem that the value of n could be averaged over a large number of samples, resulting in better resolution of the doppler. This would then allow a larger instantaneous error in the doppler measurement resulting in a higher PLO sampling rate. However, it is meaningless to sample the value of n in the register at any rate faster than the sampling rate since the value of n will not change in any time interval shorter than $1/(f_{\rm R}/R)$. Since $1/(f_{\rm R}/R)$ is 100,000 seconds and n must be sampled at rates of at least once per second (even without averaging) to obtain the required accuracy, it is seen that this technique cannot achieve the desired resolution with even practical bandwidth, let alone desired bandwidths of 300 Hz or more.

A further detrimental requirement for the configuration of Figure 3-1 is that the register containing (N+n) must contain about 38 stages in order to generate a $10^{-4}\,\mathrm{Hz}$ output frequency from a 19 MHz input frequency. The number of stages could be reduced by translation of f_s to the 19 MHz interface, however, a 30 bit divider would be required even if the interface frequency were translated to only 100 kHz. For the above reasons the programmable divider PLO is not suitable for use as a digital VCO doppler extractor.

3.1.2 ITERATIVE SYNTHESIZER

The iterative synthesizer generates an output reference frequency by multiple division and mixing (frequency summing) of a clock input frequency. Figure 3-2 shows a 6 stage (12 bit) iterative synthesizer in which each stage contains a 2 bit register and frequency divider. Five fixed clock input frequencies are required as shown in the figure. These are F and four bus frequencies of 3F, $3F+\triangle F$, $3F+2\triangle F$ and $3F+3\triangle F$. A detailed diagram of the 4th stage is shown in the boxed-in part of the figure. Depending on the value of the 2 bit number in the 4th stage of the frequency control unit (frequency register) the appropriate switch is closed to mix one of the 4 bus frequencies with the frequency output of the previous stage (or with the fundamental clock frequency for

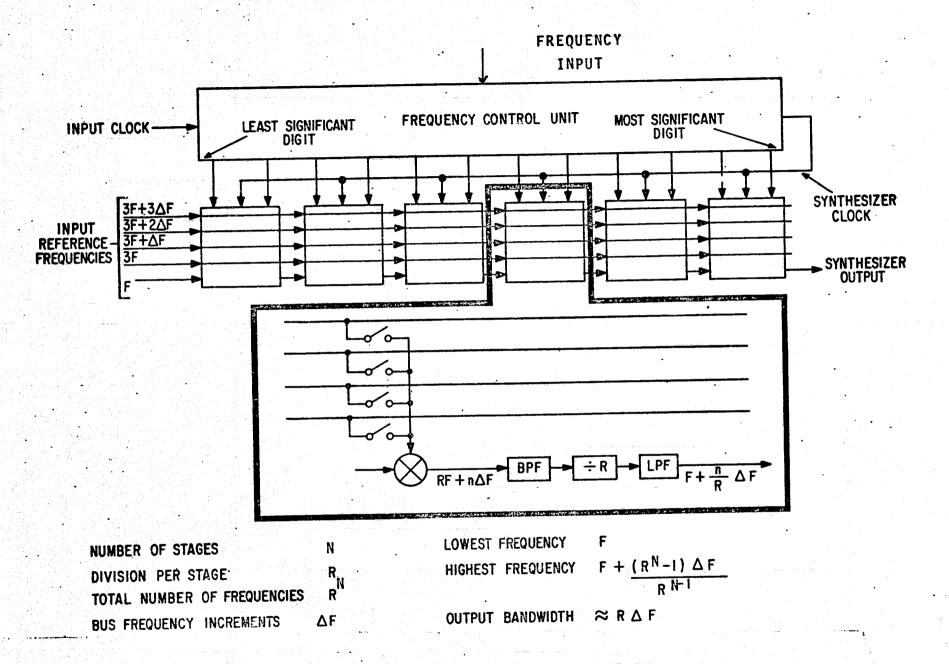


FIGURE 3-2 ITERATIVE SYNTHESIZER CONFIGURATION

1

the first or least significant stage). The sum frequency is filtered, divided by 4 (or R where R is the number of possible outputs per stage) and passed to the next stage to repeat the above process. The output frequency can be stepped in unit increments of $\Delta F/R$ from F to $\approx F+R\Delta F$ (where R is the division ratio per stage and N is the number of stages in the frequency register). The total capacity of the frequency register is Nlog₂R bits.

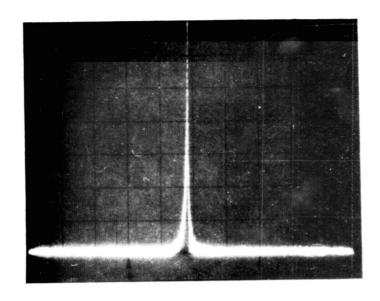
In order to track a \pm 60 kHz doppler signal to a resolution of 0.01 Hz the minimum frequency step (\triangle F/ $_R$ N-1) must be 0.01 Hz and the tuning range (R \triangle F) must be equal to 120,000 Hz. That is:

$$\triangle F = \frac{120,000}{R}$$
 $\triangle F = \frac{1}{R} = \frac{1}{R^{N-1}} = \frac{120,000}{R} = 0.01 \text{ Hz}$

Thus:
$$R^{N} = 12X10^{6}$$

If R=4 then N=12 bits, and the total capacity of the frequency register must be 24 bits. This system has been built by RCA and can meet the requirements of high resolution (0.01 Hz in 1 second), relatively wide tuning range (120 kHz) and high spectral purity. The spectrum analyzer photographs of Figure 3-3 show that this technique is capable of producing a very clean signal at RF frequencies (The frequency of the signals shown in the figure is 50 MHz). The unit could directly synthesize a 76 MHz RF output and could be phase locked to the transponder at this frequency. Thus, in terms of performance, this system is very attractive for obtaining extraction of high accuracy doppler measurements.

However, the system requires a very large amount of hardware (12 mixers, 5 clock input frequencies requiring 5 separate fixed frequency synthesizers, 48 frequency selection switches and 24 low pass filters. Figure 3-4 lists the hardware



VERTICAL - 10 dB/cm HORIZONTAL - 3 MHz/cm IF BW 3 kHz

VERTICAL - 10 dB/cm HORIZONTAL - 10 kHz/cm IF BW 1 kHz

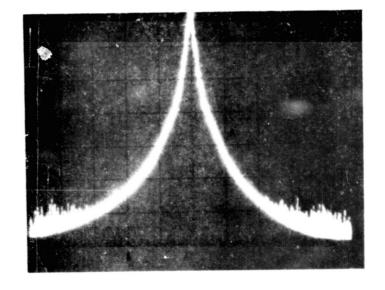


FIGURE 3-3 SPECTRUM ANALYZER DISPLAY OF 50 MHz OUTPUT

상 등장 경기 등 전 등 전 경기 등 등 등 등 등 등 등 등 등 등 등 등 등 등 등 등 등 등	DIVISION RATIO PER STAGE (R)			
PARAMETERS	2	4	8	16
REFERENCE FREQUENCIES (R+1)	2 ¹ +1	2 ² +1	2 ³ +1	2 ⁴ +1
REFERENCE FREQUENCY INCREMENTS (AF)	60 KHz	30 KHz	15 KHz	7.5 KHz
NUMBER OF STAGES FOR 2 ²⁴ (N)	24	12	8	6
NUMBER OF MIXERS (N)	24	12	8	6
NUMBER OF CROSSPOINT SWITCHES (RN)	48	48	64	96
NUMBER OF FILTERS (2N)	48	24	16	12
NOMINAL FREQUENCIES				
MIXER INPUTS				
LOWER	F	F	• F	F
UPPER	F	3F	7F	15F
MIXER OUTPUTS				
LOWER (IMAGE)	0	2F	6 F	14F .
UPPER (DESIRED)	2F	4F	8F	16F
LOWEST DESIRED FREQUENCY -	2F - β/2	4F - β/2	8F - β/ ₂	16F - β/ ₂
HIGHEST UNDESIRED FREQUENCY	F + β/2	3F + (3/8)β	7F + (7/16)β	15F+(15/32)s
GUARD SPACE	- F - ·β	F - (7/8)β	F - (15/16)8	F - (31/32)8

FIGURE 3-4 PARAMETERS RESULTING FROM VARIOUS DIVISION RATIOS

requirements for different values of R. As R increases the number of mixers and low pass filters decrease but the number of clock input frequencies increases. Thus, for space application this system is unattractive.

The amount of hardware can be reduced, somewhat, by averaging the frequency register number. For example, if the iterative synthesizer is phase locked to the S-band interface frequency with a 400 Hz loop filter bandwidth, then the frequency register could be sampled and averaged at about a 400 Hz rate. Since the standard deviation decreases as the square root of the number of samples then, over a one second averaging period, for example, the doppler error is:

where σ_{f_d} is the average doppler error over a one second period; $(\sigma_{f_d})_i$ is the instantaneous doppler error.

Since the averaged doppler error must be .01 Hz or better, the instantaneous doppler error can be 20 times largeror 0.2 Hz.

Thus:
$$\triangle F = \frac{120,000}{R}$$
but $\frac{\triangle F = \frac{120,000}{R^{n-1}} = 0.2 \text{ Hz}}{R^n}$
 $R^n = 600,000$

If R=4, then n = 10 bits and the total capacity of the frequency register must be 20 bits. However, even with this amount of averaging only 1 stage is eliminated in the iterative synthesizer and the total hardware must still consist of 10 mixers, 5 clock input frequencies and fixed frequency synthesizers, 40 frequency selection switches and 20 low pass filters.

In consideration of the amount of hardware required this technique is not considered applicable to a space hardware implementation of a digital VCO doppler extractor.

3.1.3 INCREMENTAL PHASE MODULATOR (IPM)

The principle of the incremental phase modulator is to generate a controlled frequency offset from a clock frequency f_c .

The method by which the incremental phase modulator or serradyne unit translates f_c is analogous to the well-known technique use; with traveling wave tubes for frequency translation, and thus the name is borrowed from that older technique. The principle of operation may be understood with the aid of a mechanical implementation shown in Figure 3-5. An oscillator drives a transmission line suitably matched at both ends. A sliding tap is mechanically driven over a one-wavelength (at oscillator frequency) section of the line. The motion is smooth and linear to the right, but when the end of the section is reached, the tap is very quickly snapped back to the left end. The voltage at the sliding tap output is seen to be a sine wave which exhibits a

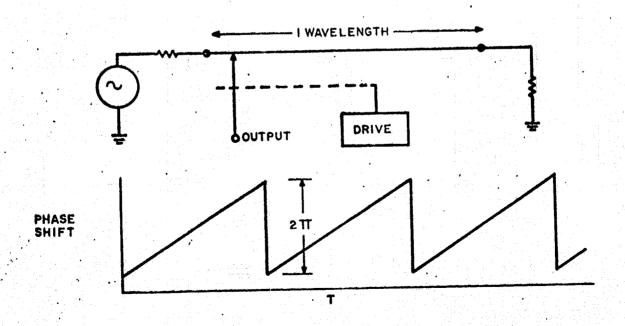


FIGURE 3-5 The Serradyne Principle

phase constantly retarding in time relative to the oscillator. Thus this output sine wave is lower in frequency relative to the oscillator by an amount exactly equal to the cycling rate of the tap motion. If the line segment is lossless and exactly one wavelength long, the motion linear, and the flyback instantaneous, then the translation is clean; there is no distortion, amplitude modulation, or spurious sidebands.

The specific way in which the serradyne unit is mechanized depends very greatly on the frequency $f_{\rm C}$, since the methods of achieving a wavelength of transmission line depend so strongly on whether $f_{\rm C}$ is in the audio or microwave region. A digital technique suitable for $f_{\rm C}$ in the neighborhood of a few MHz is illustrated in Figure 3-6. Here the oscillator output is amplified and clipped to produce a square wave, which is then applied to a delay line. The line has m taps spaced a time, T, apart such that m T is equal to $1/f_{\rm C}$. The control counter has m states (LOG₂m stages), so that after m input pulses it returns to its original position.

The counted frequency (F_R) controls the amount of frequency shift (rate of phase shift) obtained at the output and is selected digitally by the rate multiplier circuit of Figure 3-7. As it counts it causes successive taps to be selected along the line, jumping from m to 1 (or vice versa) when reaching the end. The counter is capable of going in either direction

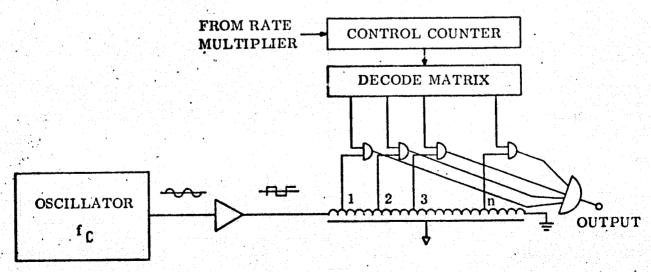


FIGURE 3-6 Serradyne Implementation

This device produces a pulse train at a rate determined by the number in the R register and a fixed frequency oscillator. If the number, R, in the R-register is thought of as having the decimal point at the left (i.e. R/Nc varies between 0 and 1), and the oscillator is at f pulses per second, then the rate multiplier output is a pulse train of $\frac{Rf_1}{N_C}$ pulses per second.

The oscillator produces a pulse train of f₁ pps which is applied to a binary counter chain of N stages, the same number as in the R-register. In this binary counter chain the carry output of each stage (lower left corner) is active when that stage undergoes a transition from the "l" to the "O" state, and it serves to trigger the succeeding stage. The rate multiplier scheme makes use of the complementary output. This output (lower right corner of each stage) shows a pulse whenever that stage goes from the "0" to the "1" state. These outputs are sometimes called "anti-carries". The anti-carries have two properties of importance here. First, the rate at which anticarries occur at the k^{th} stage of the chain is $f_1 2^{-k}$ pps. Second, an anti-carry can occur at only one of the n stages at a time. From the block diagram, Figure 3-7, if the R-register contains all zeros except a "l" in the most significant stage, then the output pulse rate is $f_1^{2^{-1}}$ pps. This occurs because the stage 1 output is $f_1/2$ and only the first "AND" gate has a high level applied to its R input. If the R register contained all zeros except a "1" in the second most significant stage, the output rate is $f_1 2^{-2}$ pps, etc. As a result of the second property of anti-carries, if both of these stages were "1", then the output rate would be f_1 (2⁻¹ + 2⁻²). In general the output rate is $\frac{R}{R}$ f, where R is the number in the register.

A caution should be observed in applying the rate multiplier to systems. The pulse rate at the output is accurate over a long period (i.e. multiples of $1/2^N f_1$ seconds), but exhibits a slightly uneven character. For example, if the R-register contains 1000---1, then most of the output pulses are spaced by $2/f_1$ seconds; but occasionally, when the N_{th} stage anticarry occurs, then a triplet of pulses spaced $1/f_1$ seconds is

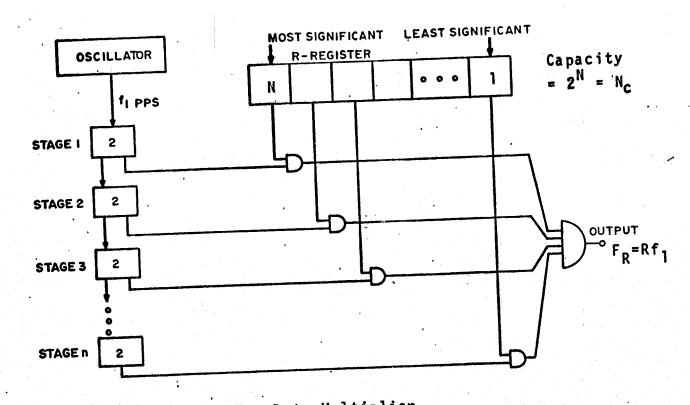


FIGURE 3-7 Rate Multiplier

(1)

observed at the output. If N is any number up to 12, the number of output pulses over a time, T, which is not necessarily a multiple of $1/f_1$, is always within one-pulse of $\frac{R}{N_c}$ 5. No better

performance could be expected, since fractions of pulses cannot occur. As N increases beyond 12, this one-pulse tolerance gradually increases, although the proportion of time that the error is greater than one-pulse is very small. The relative smoothness, expressed as a percentage of full scale, exhibits an improving trend as N is increased.

The rate multiplier output can be considered to have an algebraic sign. To do this, the R-register is arranged to represent its contents as a magnitude and sign, as one does when making hand computations. The "sign" of the output pulse rate is simply the sign associated with the R-register. The sign determines whether the phase of the clock oscillator is to be advanced or retarded.

If the rate multiplier produces a pulse rate of R f, , then the $$^{\rm N}_{\rm C}$$ output of the serradyne will be a square wave of frequency $F_{\rm C} + \frac{{\rm Rf}_1}{{\rm N}_{\rm c} {\rm m}}$. This square wave will not be smooth. This

uneveness may be reduced by making f_1 , and N (the number of stages in the rate multiplier) large.

In order to extract doppler information from the transponder signal, the incremental phase modulator can be phase locked directly to a transponder interface frequency, such as 76 MHz, as shown in Figure 3-8. In the figure, the output of the serradyne modulator (F_c) is 76 MHz and this frequency must be capable of being varied over the full doppler range (on 76 MHz). When $R=N_c$, the maximum frequency deviation of F_c is achieved and therefore

1

$$\frac{R \quad F_1}{N_{cm}} = \frac{F_1}{m} \geq 2200 \text{ Hz}$$

A typical number of taps on the delay line is m=16 so that F_1 must be 35.2 kHz. The minimum frequency change in F_c results from a one unit change in R and this must be.

$$\frac{0.01 \text{ cycle}}{27.625} = 3.62 \times 10^{-4} \text{ Hz or less. Thus,}$$

$$\triangle F = 3.62 \times 10^{-4} \text{ Hz} = \frac{F_1}{\text{m N}_C}$$
but $F_1/\text{m} = 2200 \text{ Hz}$

$$N_C = 6.1 \times 10^6 \rightarrow 23 \text{ bits}$$

With the sign bit for R the total register capacity must be 24 bits.

Doppler averaging can reduce the register capacity requirements by several bits. For example, with a 400 Hz low pass filter bandwidth, up to 400 doppler samples from the R register can be averaged over a one second period. As explained for the iterative synthesizer the doppler error is improved by $\sqrt{N_s}$ where N_s is the number of samples averaged. Thus,

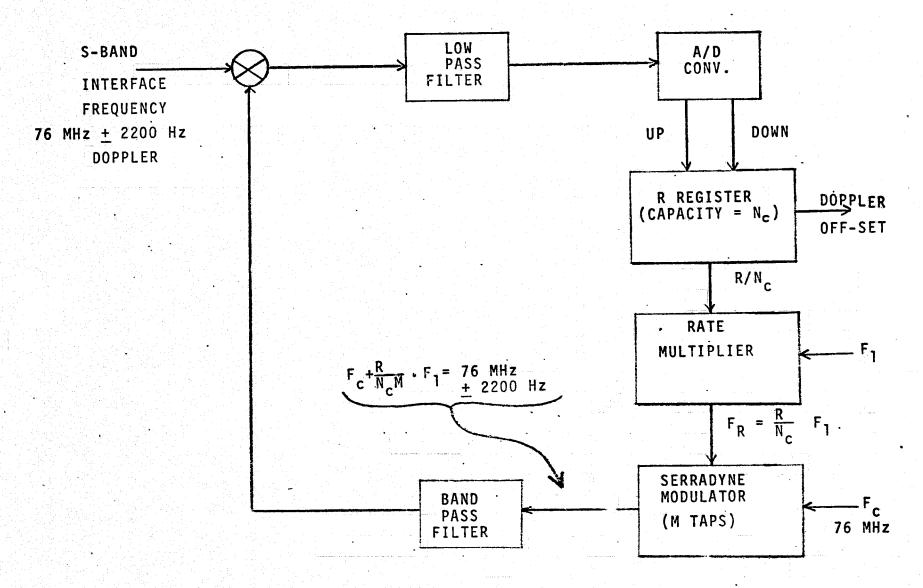


FIGURE 3-8 INCREMENTAL PHASE MODULATOR DOPPLER EXTRACTOR

$$\Delta F = \sqrt{400 \cdot 3.62 \times 10^{-4}} = \frac{F_1}{mN_c}$$

if $F_1/m = 2200 \text{ Hz}$
 $N_c = 3.04 \times 10^5 = 19 \text{ bits}$

3

1

With the sign bit the total register capacity is 20 bits.

The register capacities and frequency requirements stated above are within the hardware implementation capability. However, the incremental phase modulator still requires a rather large amount of hardware including a very stable tapped delay line. For example, the 76 MHz output from the delay line taps must be stable to at least 7.2×10^{-3} Hz in one second (assuming doppler averaging of 400 samples). This implies that the stability of the tap time delay must be no worse than 95 picoseconds $(\Delta F \times T/F_c)$ over a period T, of one second. The length of the tap delay line is $1/F_c = 13$ nanoseconds, and each tap is spaced at 822 picoseconds.

Although the IPM meets the requirements for a "reasonable" number of taps m, it exhibits excessive phase jitter. Consider a line with m = 16 taps. Phase is incremented in steps of $\frac{\pi}{8}$. Since the desired phase is uniformly distributed as a function of time over each $\frac{\pi}{8}$ phase step, the mean squared value of phase error is

$$\frac{1}{\phi^{2}} = \frac{1}{\frac{\pi}{8}} \int_{1/2(-\frac{\pi}{8})}^{1/2(\frac{\pi}{8})} \theta^{2} d\theta = \frac{\left(\frac{\pi}{8}\right)^{2}}{12}$$

Since the S/N at the output of a phase lock loop equals the inverse of the phase error variance (for S/N > 10 dB), the equivalent S/N of a signal generated by using an IPM with 16 taps is

$$\frac{S}{N} = \frac{1}{\frac{\pi}{2}} = \frac{12}{\left(\frac{\pi}{8}\right)^2} \to 18.9 \text{ dB}$$

Since the phase error as a function of time 0 (t) exhibits a sawtooth waveform, the phase noise due to phase quantization can be represented as sawtooth phase modulation of a sine wave carrier. That is,

$$\phi(t) = A \sin \left(\omega_c t + \frac{4}{m} \sum_{k} \frac{(-1)^{K-1} \sin k \omega_k t}{K}\right)$$

Thus, the phase noise consists in fact of line spectra spaced at n times the cycling rate of the delay line tap. Since line spectra are more disruptive than random phase noise, this approach is even less attractive.

To suppress the line spectra due to phase steps, the number of taps must be increased. This increases the complexity of the implementation as well as raising the switching speeds of the tap circuitry. This approach is unattractive for high accuracy doppler extraction in a flight hardware implementation.

3.1.4 ARITHMETIC SYNTHESIZER

A relatively recent approach to waveform generation and frequency synthesis makes use of the new low cost digital MSI and LSI technology. The desired output signal is generated with an all digital approach comprising an arithmetic synthesizer. This type of synthesizer constructs a set of numbers proportional to the phase of the desired signal, and converts these numbers to an analog signal with the aid of a digital-to-analog (D/A) converter. This synthesizer can be used as a direct synthesizer, or it can be followed by a phase locked multiplying loop in a direct-indirect configuration.

3:1.4.1 Direct Arithmetic Synthesizer

A block diagram of a typical arithmetic synthesizer is shown in Figure 3-9. This type of synthesizer generates a sine wave output, the frequency of which is controlled by the size of the number in the frequency register. The operation of this synthesizer is as shown in Figure 3-10. At each clock pulse the number in the register is added to the number in the accumulator. The

accumulator number grows linearly until the capacity of the accumulator is exceeded. At this point the accumulator overflows and begins to linearly increase again, in a sawtooth manner, as further register outputs are accumulated. The rate of overflow is a measure of frequency which can be controlled by changing the number in the frequency register.

To generate a sine wave output, a quadrant logic and sine function generator (ROM) could be placed between the accumulator and a D/A converter, as shown in Figure 3-9. The D/A output is a close approximation to a sine wave and the filter need only have high attenuation at the clocking frequency (to remove the staircase voltage levels out of the D/A converter). The quadrant logic converts the sawtooth variation of the accumulator output to a bi-polar triangularly warying output. This is accomplished by either accepting the accumulator output as it appears, or by complementing the number as shown in Figure 3-Ju. The complement of a linearly increasing number is a linearly decreasing number. The sine function generator converts each accumulator output to a number proportional to the sine of the accumulator output. The numerical output of the sine function generator is then fed to the D/A converter which produces a sine wave output voltage. The output low-pass filter removes the staircase sampling levels and produces a relatively clean sine wave output frequency.

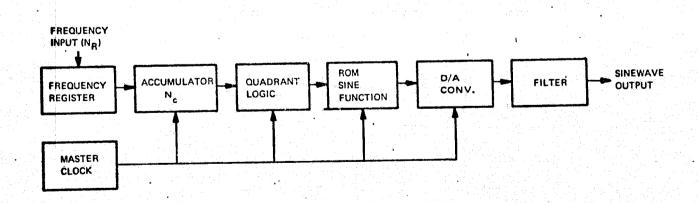
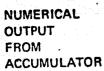
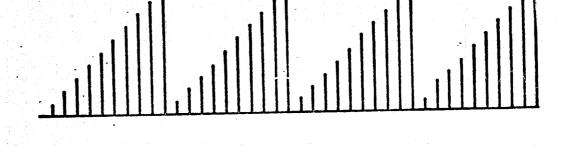


FIGURE 3-9 An Arithmetic Synthesizer



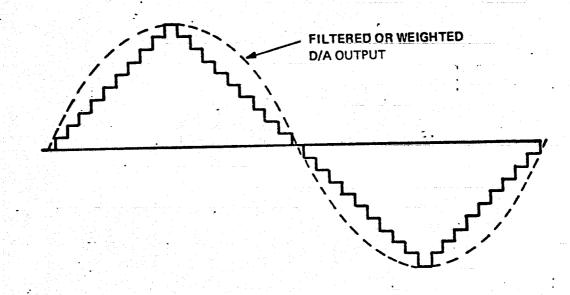


QUADRANT LOGIC POSITIVE COMPL OF NUMBER OF NUM

COMPLEMENT OF NUMBER

NEGATIVE OF NUMBER NEG. COMP. OF NUMBER



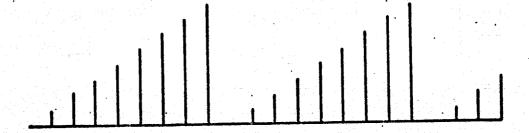


Alternatively, the output of the accumulator could be fed directly to a linear digital-to-analog converter (D/A) with the result that the output signal would be a staircase voltage similar to a sawtooth signal. The output filter would then need high attenuation at harmonics of the fundamental frequency. However, the quadrant logic and sine function ROM would not be required. With this alternative approach the arithmetic synthesizer output would appear as shown in Figure 3-11.

For the direct sawtooth output, the output frequency of the synthesizer is related to the number in the register (N_R), the accumulator capacity (N_C), and the clock frequency (F_O) through the expression:

$$F_S = \frac{N_R}{N_C} F_O$$

MAGNITUDE OF COUNT OUT OF ACCUMULATOR



STAIRCASE OUTPUT OF D/A CONVERTOR. UNFILTERED AND FILTERED

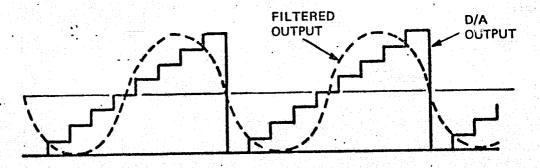


FIGURE 3-11 Arithmetic Synthesizer Waveform Generation.

Since the accumulator sums several values of N_R before overflow, then $N_R < N_c$ and $F_S < F_o$. However, the accumulator is adding N_R at the clock rate, and for present logic speeds the clock rate should not exceed about 10 MHz. Since the synthesizer frequency is less than the clock frequency it is not practical, with present logic, to generate synthesizer frequencies in excess of a few megahertz. To generate RF frequencies at VHF or higher, the arithmetic synthesizer frequency can be multiplied by a factor K, such that the RF output frequency is KF_S . This could be accomplished with a multiplying phase locked oscillator as shown in the block diagram of Figure 3-12. Thus, in terms of the arithmetic synthesizer parameters, the RF output frequency is given by:

$$\mathbf{F}_{\mathbf{RF}} = \mathbf{K} \frac{\mathbf{N}_{\mathbf{R}}}{\mathbf{N}_{\mathbf{C}}} \mathbf{F}_{\mathbf{0}}$$

where K is the frequency multiplying ratio.

Since N_R , N_c and K are integers, only discrete RF frequencies can be generated for a fixed clock frequency. However, the number and accuracy of these frequencies can be selected to any desired degree by proper selection of the multiplying ratio, the accumulator capacity and the clock frequency. Since the smallest change in the RF frequency (assuming N_c , K F_o are fixed) results from a \pm 1 change in N_R , then this smallest RF frequency change (or channel spacing is given by:

$$\Delta F_{RF} = \frac{K F_o}{N_c}$$

If the transponder interface frequency is 76 MHz, if the clock frequency is 5 MHz and if the arithmetic synthesizer output frequency is 1 MHz, then K is 76. For a .01 Hz frequency change at S-band, or 3.62X10⁻⁴ Hz change at 76 MHz, the accumulator capacity must be:

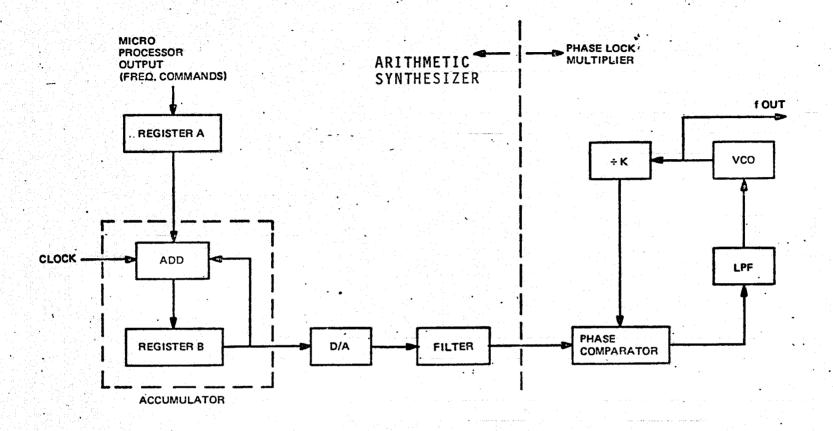


FIGURE 3-12 FUNCTIONAL BLOCK DIAGRAM OF AN ARITHMETIC SYNTHESIZER

$$3.62 \times 10^{-4} = \frac{76(5 \times 10^6)}{N_c}$$

or
$$N_c = 1.05 \times 10^{12} \rightarrow 40$$
 bits

However, as the discussion of doppler extraction which follows will show, the accumulator capacity can be reduced far below this value if the phase information is used to extract the doppler information. It will be shown that the capacity need only be 20 bits or less to extract doppler off-sets to 0.001 Hz in a one second time interval. This is due to the fact that the arithmetic synthesizer contains accurate phase information (to one part in 10^6 for $N_{\rm C}$ = 20 bits) even though the instantaneous frequency is only resolved to one part in 10^6 .

The advantages of using an arithmetic synthesizer to generate desired frequencies include unlimited frequency and phase resolution (determined by the capacity of the accumulator), phase continuity when frequency is changed, simple and direct frequency switching (only the number in the frequency register is changed), and rapid and precise control of frequency and phase during switching operations. The latter advantages are of added importance when the synthesizer is to be used to track rapidly changing frequencies. For example, an arithmetic synthesizer can settle to a new frequency in a few microseconds or less, determined in part by the clocking rate and the settling time of the D/A converter. Other advantages include the ability to place the entire arithmetic portion on one or two LSI chips with the result that the synthesizer weight, size and power consumption can be made very small.

The primary disadvantages of the arithmetic synthesizer of Figure 3-9 are the inability of the synthesizer to operate above a few megahertz without using very high speed logic circuits, spurious signals introduced by the accumulator overflows, and the quantization noise added by the finite resolution of the D/A converter.

The first disadvantage is overcome with the use of the multiplying phase locked oscillator but this also multiplies the spurious levels causing them to be a serious problem. For narrow band applications, however, the spurious signals can be reduced to very low values by proper selection of the synthesizer output frequency. Figure 3-13 shows a typical D/A output time signal with a high level spurious signal clearly shown. The particular spurious signal shown in the figure $(0.07\ F_0)$ is far removed from the desired signal $(0.31\ F_0)$. However, at certain frequencies, this spurious signal could be within the bandpass of the output filter. In the example shown, the unfiltered spurious signal is only 10 dB below the desired output signal.

Typical spurious levels are shown in the actual spectrum analyzer photographs of Figure 3-14. As shown in the figure, some frequencies generate very clean spectra (particularly when the ratio of synthesizer frequency to clock frequency is equal to the ratio of two small integers), while others produce spectra with very high level and close in spurious signals. Thus, a very clean spectrum can be obtained if the synthesizer frequency is chosen close to an integer ratio of the clock frequency. The total doppler excursion only represents a frequency deviation of \pm three parts in 10^5 or .003%. Thus the full doppler shift can be obtained by only a very slight deviation of the synthesizer from a sub-harmonic of the clock frequency.

The quantization noise from the D/A converter also adds to the noise level. For example, a typical 10 bit D/A converter will cause voltage distortions of approximately \pm 0.05%, resulting in a signal-to-noise output of the synthesizer of about 60 dB. Higher resolution D/A converters are available but the cost increases rapidly with increasing resolution. A 12 bit D/A converter would increase the S/N level to 72 dB. Also, the VCO loop filter will reduce the noise below this level but the frequency multiplication will raise it.

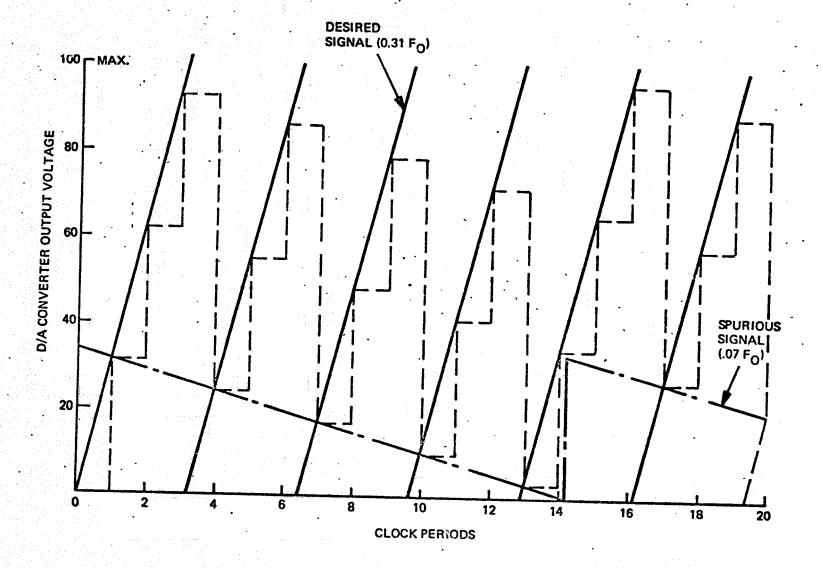
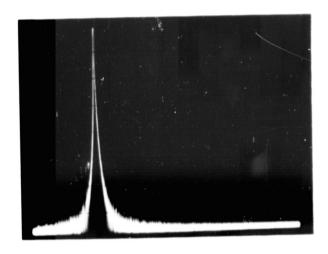
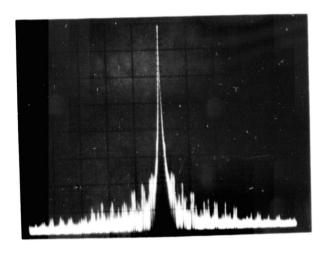


FIGURE 3-13. TYPICAL D/A OUTPUT SIGNAL

1. 187.5 KHz (3/16 FO) 5 KHz/DIV 30 Hz MEASUREMENT BW



2. 200.001 KHz
 5 KHz/DIV
 30 Hz MEASUREMENT BW



3. 212.501 KHz 5 KHz/DIV 30 Hz MEASUREMENT BW

Fo = 1 MHz Nc = 16 BITS

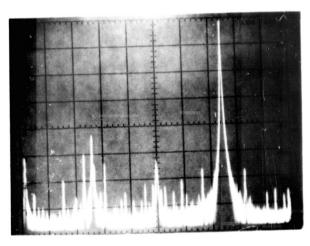


Figure 3-14. Typical Spectra of An Arithmetic Synthesizer

3.2 DIGITAL VCO SELECTION DECISION

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From the discussions of the previous paragraphs, the arithmetic synthesizer offers the best performance with the least circuit complexity and is recommended as the technique to be used for designing a digital VCO doppler extractor. The digital operations of the arithmetic synthesizer can easily be placed on one or two LSI chips offering the potential for a low weight, low power and high reliability DVCO. The programmable divider DVCO cannot be employed in a high accuracy doppler extractor since the bandwidths required for this unit are too narrow to be practical. The iterative synthesizer could meet the accuracy and bandwidth requirements for the doppler extractor, however, it is far too complex for a flight hardware system. The incremental phase modulator could also meet the requirements, provided the spurious levels could be reduced, however, this technique also requires highly complex circuitry and high stability components. Only the arithmetic synthesizer offers high accuracy and sufficient bandwidth, combined with relatively simple circuitry. The fact that only the arithmetic synthesizer has an easily accessible measure of RF phase (in the accumulator register) also makes this technique attractive for extracting range or changes in range to very high accuracy.

SECTION 4

DVCO DOPPLER EXTRACTOR ANALYSIS

4.1 EXTRACTION OF DOPPLER USING THE ARITHMETIC SYNTHESIZER

To extract doppler information, the arithmetic synthesizer can be phase locked to the 76.083 MHz output of the S-band transponder as shown in Figure 4-1. A multiplying VCO is used to multiply the low frequency arithmetic synthesizer output up to the 76.083 MHz interface. The VCO is phase locked to the arithmetic synthesizer frequency through the inner loop comprising the : K and phase detector unit. This is assured by making the inner loop filter wide band and hence with faster phase error correction. The arithmetic synthesizer is phase locked throughthe outer narrowband loop comprising the register, accumulator, D/A converter, phase detector, wide band filter and VCO. register is not set at the appropriate frequency, the VCO will not be tuned to exactly 76.083 MHz. Thus, an error signal will be generated which will bring the register to the correct number through the A/D converter. The VCO will follow the arithmetic output of the accumulator to bring the arithmetic synthesizer and VCO into phase lock with the 76.083 MHz input frequency.

At phase lock the doppler signal could be obtained directly from the register number since this number follows the 76.083 MHz output frequency in a linear manner. However, since phase jitter, very short term frequency stabilities and doppler rates will cause the register number to vary significantly, a means of averaging the register values over the desired averaging period would improve the accuracy of the doppler measurements and reduce the requirements for the register capacities.

As was discussed previously, 40 bit registers would be required if the instantaneous doppler frequency is to be measured to a 0.01 Hertz resolution. The frequency register values could be averaged over the desired averaging period. This could be accomplished by periodically transferring the frequency register contents to a large accumulator. After the desired

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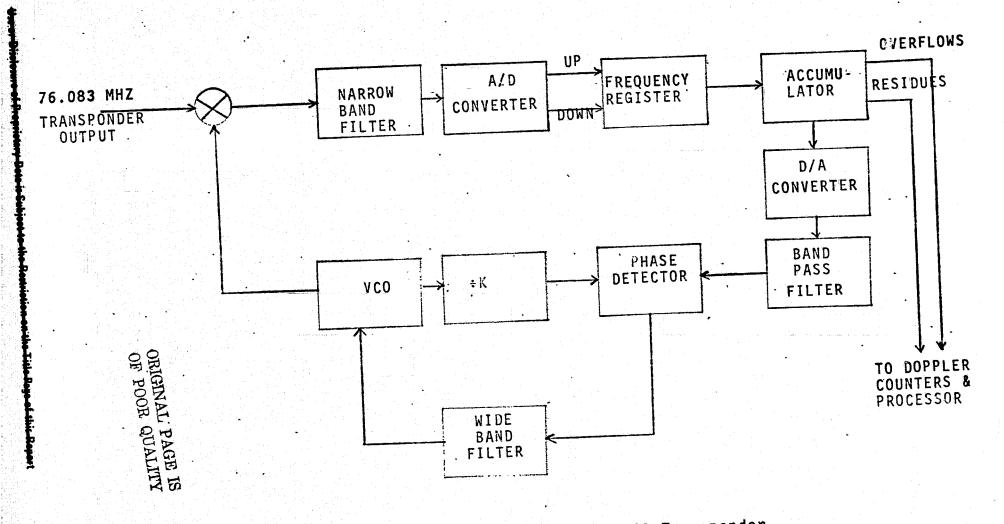


Figure 4-1. Doppler Extraction From a USB Transponder

integration period has elapsed the accumulated frequency counts could be transferred to the computer, along with the account of the number of times the frequency register contents (clock counts) was transferred to the accumulator. The ratio of these two counts, would result in a measure of the doppler shift.

The averaging process described above can be accomplished without the need for a separate averaging accumulator since the accumulator register in the arithmetic synthesizer is accomplishing the averaging of the frequency register values. Thus, by counting the number of overflows in the phase accumulator, and using the residue values at the start and stop of each integration interval, the doppler averaging is accomplished with very little additional hardware. Figure 4-2 shows a block diagram of the technique to extract doppler from the phase accumulator values. The frequency of the arithmetic synthesizer is defined by the rate of accumulator overflow and is nominally equal to the 76.083 MHz input frequency divided by the VCO divisor (K). Thus, in counting the overflows over a known time interval the input frequency and its doppler component can be calculated.

The operation of the counters and extraction of the input frequency is shown in the timing diagram of Figure 4-3. The overflow counter begins counting accumulator overflows at the first overflow following the start command and ceases its count at the last overflow preceding the stop command. The clock counter begins counting the clock frequency from the start to the stop command. The start and stop commands will start and stop the counters at the clock signals immediately following the commands. Thus, the time interval will be measured exactly. A small start and stop time delay (lock period) may occur if the start and stop commands are not synchronous with the clock signals. The clock signals are the exact times that the accumulator is updated by the register number so that the instantaneous accumulator value is an exact measure of the instantaneous sawtooth envelope phase.

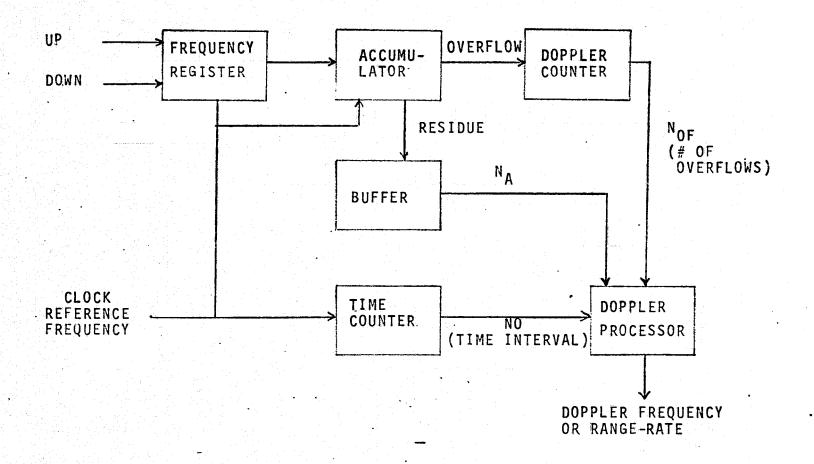


FIGURE 4-2. Doppler Counters and Processor

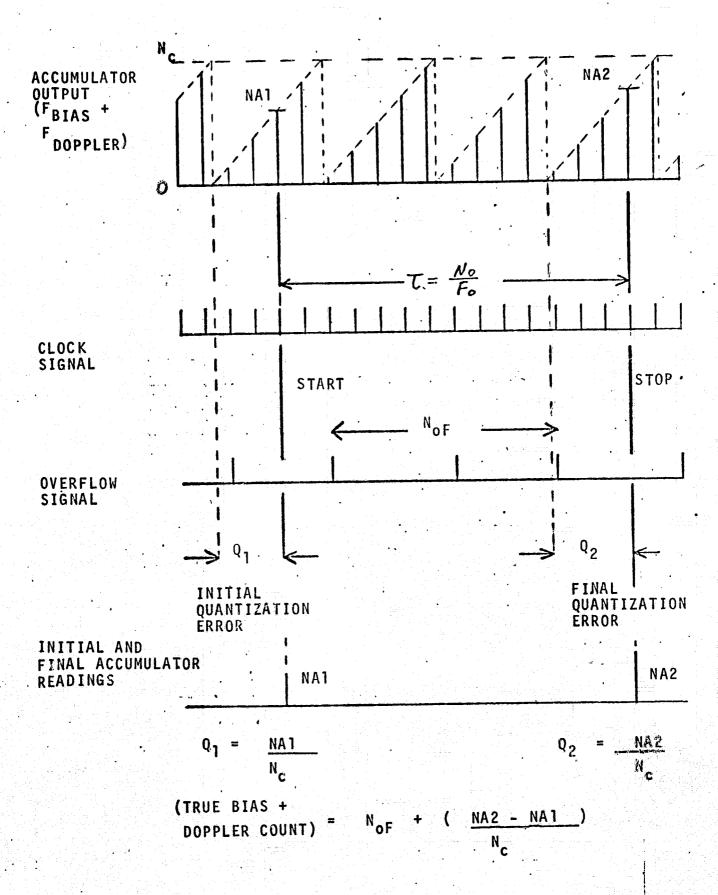


FIGURE 4-3 Timing Diagram for Doppler Extraction

If $N_{\mbox{of}}$ is the overflow count and $N_{\mbox{o}}$ is the clock count over an integration time t, the arithmetic synthesizer frequency is:

$$F_s \approx \frac{N_{of}}{t} = \frac{N_{of}}{N_o}$$
 F_o

where Fo is the clock frequency

However, the overflow count has a quantization error at the beginning and end of the integration period. As shown in Figure 4-3, the quantization error is referenced to zero phase of the accumulator sawtooth envelope. Since phase is linearly proportional to the accumulator value the quantization error can be derived from the accumulator values at the start and stop commands. The portion of a sawtooth cycle completed is $\rm N_a/N_C$ where $\rm N_a$ is the accumulator value and $\rm N_C$ is the accumulator capacity. From Figure 4-3, the overflow signal represents the completion of a sawtooth cycle. The accumulator values at the start and stop commands are read into a buffer and are used to calculate the quantization correction to the overflow count. The exact arithmetic synthesizer frequency is determined by the relationship

$$F_{Synth} = \frac{\left(N_{of} + \frac{N_{a2} - N_{a1}}{N_{o}}\right) F_{o}}{N_{o}}$$

where $N_{of} = overflow count$

 N_{a2} = accumulator residue at the stop command

 N_{al} = accumulator residue at the start command

 $N_0 = clock count$

F = clock frequency

The frequency of the received S-band transponder signal is (assuming a nominal 2101.802 MHz S-band frequency and multiplication of the arithmetic synthesizer frequency to a transponder interface frequency):

$$F_{S \text{ band}} = K \cdot \frac{2101.802}{76.0833} \cdot F_{synth}.$$

$$F_{S \text{ band}} = 27.625K \left[\frac{N_{0F} + \frac{N_{a2} - N_{a1}}{N_{0}}}{N_{0}} \right] F_{0}$$

where K is the value of the VCO frequency divisor.

The doppler shift, referenced to the S band frequency, is:

$$F_{doppler} = 27.625K \left[N_{OF} + \frac{N_{a2} - N_{a1}}{N_{C}} \right] \cdot \frac{F_{O}}{N_{O}} - 2101.8020833 \text{ MHZ}$$

4.2 ERROR ANALYSIS

An analysis of the doppler measurement errors associated with using the arithmetic synthesizer DVCO was made. The major error sources are the quantization error resulting from a ± 1 count error in the numbers in the digital registers, the phase jitter resulting from any noise in the loop filters, and frequency drift errors caused by short term frequency instability in the clock reference oscillators. As the analysis shows, the quantization error can be reduced to any desired level by choosing large enough capacities in the frequency and accumulator registers. The phase jitter, primarily caused by spurious signals on the DVCO output, is the largest error source when a high stability clock is used. However, this error source can be reduced to acceptable levels by proper selection of the operating frequencies and the S-band transponder interface technique. A description of each error source and its impact on the total error budget follows.

4.2.1 DVCO QUANTIZATION ERROR

The doppler shift on the arithmetic synthesizer frequency is derived from the accumulator overflow and residue counts by the formula

$$F_{d_A} = \frac{\begin{bmatrix} N_{of} + \frac{N_{a2} - N_{a1}}{N_{c}} \\ \frac{N_{c}}{t} \end{bmatrix}}{T}$$

where $F_{dA} = doppler$ shift in the arithmetic synthesizer frequency.

Nof = overflow count

 $N_{a,2}$ = accumulator residue at the stop command

 N_{al} = accumulator residue at the start command

t = integration period

F_B = nominal zero doppler arithmetic synthesizer frequency

The ratio N_a/N_c (i.e. N_{a2}/N_c or N_{a1}/N_c) represents the fraction of a cycle that is to be added to the whole cycle count (N_{of})

to resolve the nominal \pm 1 count error in N_{of} . The fractional cycle count, however, contains a \pm 1 count error that results in a small quantization error in the computed synthesizer frequency (F_A) . The resultant quantization error in the doppler frequency, resulting from a \pm 1 count error in N_a , is given by:

$$\varepsilon_{FdA} = \frac{+}{N_c t}$$

This error is uniformly distributed over the above limits and thus has a standard deviation given by:

$$\int_{\mathbf{F}} \mathbf{d_A} = \frac{1}{N_c + \sqrt{6}}$$

The actual doppler shift on the arithmetic synthesizer must be multiplied by the ratio of the S-band doppler to the arithmetic synthesizer doppler. The resultant multiplication also multiplies the doppler error, so that, referenced to the S-band doppler, the quantization error is:

$$\int Fd = \frac{R}{N_c t \sqrt{6}}$$

referenced to S band

A second source of doppler quantization error exists due to the quantized values of frequency in the frequency register (N_R). The arithmetic synthesizer can only generate discrete frequencies whose values are,

$$F_S = \frac{N_R}{N_C}$$
 F_o

where N_R is a variable.

 N_R can change by no less than 1 unit so that F_S can only change by F_o/N_c . At the S-band frequency ($F_t = RF_s$), the minimum frequency change is R_o/N_c . However, if the S-band frequency (at 2101.8 MHz for example) is half way between two possible frequencies from the arithmetic synthesizer, then N_R should take on half unit values. That is:

$$F_S$$
 band = $R(F_S + \Delta F_S) = R \frac{N_R + 1/2}{N_C} F_O$

But N_R can not be changed by 1/2 count. The S-band frequency, however, can still be tracked by the closed loop system of Figure 4-1, if N_R is periodically increased and reduced by one count. That is N_R would periodically take on values of N_R , N_R+1 , N_R , N_R+1 , etc. such that the average value would be $N_R+1/2$.

However, the overall bandwidth of the loop filter will restrict N_R from changing at a rate significantly faster than the bandwidth. Thus, N_R will remain at one of the two values indicated above for a period of approximately $1/B_L$ (inverse of the loop bandwidth). The accumulator will accumulate the values of N_R causing the overflows to occur sooner or later than the true reference zero crossings. The frequency error, referenced to S-band will be $\Delta F = \frac{1}{2} \frac{RF}{0}$ over short periods of time ($\approx 1/B_L$).

The phase error between the true S-band signal and the synthesizer frequency (referenced to S-band) will increase linearly with time until N_R is reduced by one count. At this time the phase error will decrease linearly until a maximum negative phase error is achieved. The phase error will thus vary linearly with time with a triangular waveform of frequency $\approx B_L$. The maximum amplitude of the phase error will be:

$$\phi_{\epsilon} = \pm \frac{\Delta F}{2 B_L} = \pm \frac{RFO}{4 N_c B_L}$$
 cycles

This phase error will cause a doppler frequency error since the overflow count (N_{oF}) will be in error from the true S-band signal by the above amount of phase error. Thus, the maximum doppler error will be

$$\xi_{Fd} = \frac{\phi_{\varepsilon}}{t} = \frac{+}{4} \frac{RFO}{4 N_c B_L t}$$

The standard deviation is given by

$$\mathbf{T}_{\mathbf{d}} = \frac{\mathsf{RFo}}{4\mathsf{N}_{\mathbf{G}} \mathsf{B}_{1} \mathsf{t} \sqrt{6}}$$

The above error source is seen to be dependent on both the accumulator capacity (N_c) and the overall loop bandwidth (B_L).

Thus, it can be reduced not only by making the accumulator capacity large but also by selecting a wide loop bandwidth.

Comparing this quantizing error source with the error resulting from the quantized residue counts indicates that the former is $F_0/4B_1$ times the latter. Since the clocking rate (F_0) must be much larger than the loop bandwidth, the quantizing error resulting from an error in N_{R} is much larger than the error resulting from the quantized residue values. Assuming that a clocking rate of 5 MHz is typical, and a minimum loop bandwidth of 335 Hz has been selected then $F_{\rm o}/4B_{\rm c}$ is equal to 3731. is, the doppler error resulting from an error in N_{R} could be almost 4000 times larger than the doppler error resulting from an error in Na.

The above bandwidth was selected only as an example. Since other error sources to be discussed, such as noise induced phase jitter and doppler rate tracking error, are also sensitive to loop bandwidth, a trade-off of loop bandwidth is necessary for a minimum This trade-off will be discussed after the other error system. error sources have been defined.

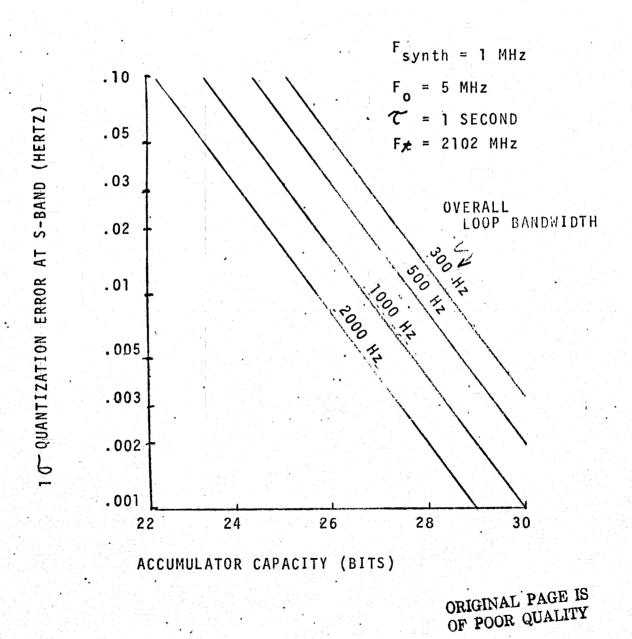
The quantization error for a fixed accumulator capacity depends on the interface used with the S-band transponder. Conversely, the quantization error can be made arbitrarily small, provided an adequate number of bits are carried in the accumulator. The required accumulator capacity for various transponder interface implementations will be explored.

4.2.1.1 Multiplication of DVCO Frequency to the Transponder Interface Frequency

If the arithmetic synthesizer frequency is multiplied directly to the interface frequency, then R has a value given by:

$$R = \frac{F_{Sband}}{F_{arith synth}} = \frac{F_{t}}{F_{A}}$$

The primary quantization error, resulting from a ± 1 count error in N_R , results in an S band doppler error given by:



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FIGURE 4-4 QUANTIZATION ERROR FOR DIRECT MULTIPLICATION
TO AN S-BAND FREQUENCY.

$$\sigma_{Fd} = \frac{R F_0}{4N_C B_1 t \sqrt{6}} \equiv \frac{F_t F_0}{4N_C F_A B_L t \sqrt{6}}$$

This error is independent of the interface frequency, and is also the error resulting when the synthesizer is used as a transponder VCO reference frequency. (That is, direct multiplication of F_A to the S band frequency through multipliers and IF mixers).

with the clock frequency (F_0) equal to 5 MHz and the S band frequency (F_t) equal to 2102 MHz, Figure 4-4 shows the trade-offs of register capacity and loop bandwidth to achieve various doppler error bounds. The synthesizer frequency (F_A) is assumed to be 1 MHz and the averaging period (t) is 1 second for the results shown in the figure. It is seen from the figure that an accumulator capacity of from 26 to 28 bits is required to reduce the worst case quantization error to 0.01 Hz or less.

Since $F_A = (N_R/N_c)F_0$, then the error equation can also be written as

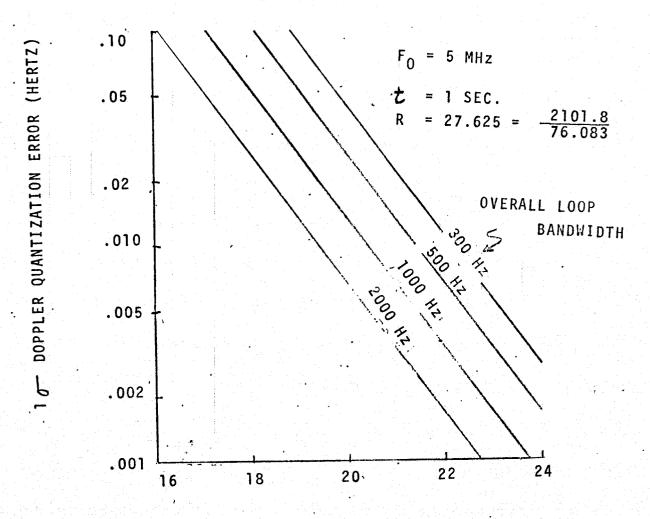
$$^{\circ}$$
Fd = $\frac{F_{t}}{4N_{R}B_{L}t\sqrt{6}}$

Assuming F and , are fixed at some desired values, then the doppler quantization error can only be reduced by increasing the frequency register number (and hence the accumulator capacity) or by increasing the overall loop bandwidth.

4.2.1.2 Translation of DVCO Frequency to the 76 MHz Transponder Interface Frequency

If the DVCO frequency is translated to the 76 MHz interface frequency then R is reduced by several orders of magnitudes. This will also reduce the quantization error proportionately, or reduce the register capacity requirements. In the frequency translation technique R has a value given by:

$$R = \frac{F_{Sband}}{F_{VCO} \text{ (transponder)}} = \frac{2101.8}{76.083} = 27.625$$



ACCUMULATOR CAPACITY (BITS)

FIGURE 4-5 QUANTIZATION ERROR FOR DVCO TRANSLATION
TO THE 76.083 MHz INTERFACE.

ORIGINAL PAGE IS OF POOR QUALITY The doppler quantization error is then:

$$\sigma_{\text{Fd}} = \frac{27.625 \, F_{\text{o}}}{4N_{\text{c}} \, B_{\text{L}} \, t \, \sqrt{6}}$$

With a 5 MHz clock (F_0) and a one second integration period (t), the resultant quantization error is shown in Figure 4-5, as a function of loop bandwidth and accumulator capacity. With the translation of the DVCO frequency, the capacity of the accumulator is reduced to about 20 to 22 bits. Comparing Figure 4-5 with Figure 4-4, it is seen that the capacity of the accumulator is reduced by about 6 bits for the same loop bandwidth. Alternatively, the translating technique allows the use of much narrower loop bandwidths for the same quantization. As will be shown, narrow loop bandwidths are desired to reduce loop noise levels so that the translating technique will be desirable both for low quantization noise and low noise induced doppler errors. However, as was shown, the loop bandwidths cannot be made narrower than about 335 Hz for accurate tracking of doppler rates.

4.2.2 FREQUENCY STABILITY ERRORS

The DVCO converts a clock reference frequency to a desired DVCO frequency by the arithmetic operations of the accumulator. Assuming these arithmetic operations (accumulation of digital numbers) are error free and since they are stable, the short and long term stabilities of the DVCO frequency is the same as the clock reference frequency. This arises in part from the linear and stable conversion of clock phase to DVCO phase and by the definition of error sources. That is, any additional frequency instabilities on the DVCO can be traced to other error sources, such as described previously, or those caused by noise or other phase fluctuations in the feedback loop of Figure 4-1. Thus, the equations for doppler error discussed in Volume I apply. That is, the doppler error resulting from instabilities in the clock frequency is defined as:

$$F_d = S \cdot F_t$$

where S is the RMS short or long term stability factor for the clock reference oscillator and $F_{\mathbf{t}}$ is the S-band transmitter frequency. This error source is independent of the technique for interfacing the doppler extractor with the S-band transponder provided all injection frequencies and mixer output signals are as clean, proportionate to the frequency, as the clock reference. The above doppler error applies to any well designed doppler extractor regardless of the transponder interface technique.

To achieve a maximum 1 σ doppler error of 0.01 Hz at S-band (2 GHz) requires a clock stability of 5×10^{-12} or better. This stability is within the present state of the art for flight hardware so that a doppler error of 0.01 Hz is feasible in a practical system.

4.2.3 NOISE INDUCED DOPPLER ERRORS

With noise present in the phase locked loops of Figure 4-1, a phase jitter exists on the VCO output frequencies. As discussed in Volume 1 and Reference 1, the phase jitter results in a doppler measurement error that depends on the S/N ratio in the loop filter. This doppler error is given by:

$$F_{d} = \frac{R}{2 \pi t \sqrt{(S/N)_{Loop}}}$$
 (Referenced to S-band)

where T is the doppler averaging period and $(S/N)_{Loop}$ = loop signal to noise ratio, R is an error multiplying constnat that depends on the transponder/doppler extractor design and the noise source.

Two sources of noise exist; namely noise sources external to the phase lock loops and noise sources internal to the loops. Any external noise source, such as RF input noise, is reduced in part by the loop gain. This was shown in Volume 1 where the doppler error resulting from a loop S/N value was independent of the transponder interface technique. That is, R equals 1 in the above equation for

an external noise source, independent of the interface technique. Thus the doppler error is:

$$\mathcal{O}_{F_d} = \frac{1}{2\pi t \sqrt{S/N} Loop}$$

where (S/N) loop is the loop S/N ratio resulting only from an external noise source such as RF noise.

Since the S/N ratio improves as the loop bandwidth is made narrower, this error can be reduced by selecting a loop bandwidth as narrow as possible. Other error sources, however, may increase above the noise induced errors if the loop bandwidth is made too narrow. To obtain a one sigma doppler error of .01 Hz or less in one second of averaging, the loop signal to external noise ratio must be greater than 24 dB.

Noise sources that are internal to the loop, such as VCO phase noise at frequencies higher than $\omega_{\rm h}$, and spurious signals that arise from the DVCO process, will not be reduced by the loop gain, and in fact, will be increased if a frequency multiplication occurs in the loop.

The primary sources of internal DVCO noise are the amplitude distortions resulting from the quantized voltage error out of the D/A converter and the spurious signals generated by the arithmetic processes in the accumulator. The following paragraphs discuss each of these noise sources and their impact on the total noise level (and hence the doppler accuracy) in the loop bandwidth.

4.2.3.1 D/A Quantization Noise

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One source of internal phase noise is the quantized voltage steps due to the finite voltage resolution of the D/A converter and the accumulator outputs. Each of these noise sources produces a quantized voltage error which could be as large as one least significant bit in the quantizing source. That is, the signal to noise ratio due to D/A quantization is:

$$(S/N)_{D/A} = (2^N)^2 = 2^{2N}$$

where N is the bit capacity of the D/A converter. Likewise, for the accumulator output the S/N level is:

$$(S/N)_{ACC} = (2^m)^2 = 2^{2m}$$

where m is the bit capacity of the accumulator. Since the accumulator capacity is often much larger than the D/A capacity (20 to 30 bits for an accumulator versus 10 to 16 bits for the D/A converter), the output S/N is primarily due to the D/A converter. Reference 11 discusses D/A noise and mentions that the quantized noise is distributed over the bandwidth of the signal. Assuming the quantized levels are distributed uniformly over \pm 1/2 of the least significant bit, and since they are changing randomly at the clocking rate, the noise spectrum will be approximately uniformly distributed over the frequency range from DC to the clock frequency plus the synthesizer frequency [($F_0 + F_s$) = F_0 if $F_S \in F_0$].

Thus, the S/N ratio out of the D/A converter will be

$$(S/N)_{D/A} = 2^{2N}$$

with the noise distributed in frequency from zero to F_0 .

The bandpass filter on the D/A output will reduce this noise level approximately by the ratio of the filter bandwidth to the clock frequency.

Or $(S/N)_{D/A}$ (filtered) = 2^{2N} $(\frac{F_0}{B_E})$

where B_F is the bandwidth of the bandpass filter. If the synthesizer frequency is multiplied by K with a narrowband multiplying phase locked loop, then the S/N will decrease by K^2 . However, the narrowband filtering of the phase lock loop will increase the S/N ratio with B_L (the loop bandwidth) replacing B_F in the above expression. The resulting loop S/N ratio, after multiplication will be:

 $(S/N)_{100p} = 2^{2N} \left(\frac{F_0}{B_1}\right) \frac{1}{\kappa^2}$

Reference 11 - STEIN AND JONES, "Modern Communication Principles"
Mc-Graw-Hill 1967 Pages 205 to 209.

To obtain an idea of the loop S/N ratio due to D/A noise, the following typical parameters are assumed.

 $F_0 = 5 MHz$

 $B_1 \simeq 500 \text{ Hz}$

N = 10 bits (DA Converter Capability)

Then, if K = 1, the loop S/N ratio is:

$$(S/N)_{100p} = 1.05 \times 10^{10} = 100 \text{ dB}$$

If K has a value of 100, the S/N is reduced 40 dB to a loop S/N ratio of 60 dB. A 12 bit D/A will increase each of the above S/N ratios by 12 dB. Narrower loop bandwidths will also increase the S/N ratio inversely to the value of the loop bandwidth. Thus, with narrow band filtering it is possible to raise the loop S/N ratios to acceptable levels, provided K is not too large.

4.2.3.2 Spurious Signals Generated in the Digital VCO

The arithmetic synthesizer and many other types of digitally controlled VCO's generate spurious signals whose magnitude, frequency and number of spurii depend on the ratio of the clock and synthesizer frequencies. As the photographs of Section 3. have shown, if the clock frequency is a harmonic of the synthesizer frequency, a very clean spectral signal is obtained.

The diagrams of Section 3 have also demonstrated that the spurious signals result from variable overflow residues in the phase accumulator. If the residue value is constant, no spurious signals will occur. However, the residue value is constant only if the accumulator capacity is an integer multiple of the frequency register number (N_p) . That is:

$$N_c = M \cdot N_R$$

where M is an integer.

The instantaneous value in the accumulator is given by:

$$N_{ai} = N_{ao} + \sum_{i} N_{Ri}$$

where N_{ai} = instantaneous value in the accumulator

 N_{ao}^{-} initial value in the accumulator

 N_{Ri} = instantaneous value in the frequency register

Assuming N_{Ri} is constant, then after M summations of N_{R} the value of Nai will be

$$N_{ai} = N_{ao} + MN_{R} = N_{ao} + N_{c} = N_{ao}$$

However, the synthesizer frequency is $(N_R/N_C)F_0$. $N_R/N_c = 1/M$ then:

$$F_s = F_o$$

 $F_0 = MF_s = harmonic of the synthesizer frequency.$ or

The spurious signals that are generated can be determined mathematically from a series of modulo calculations between the register number and the accumulator number. The frequency of the spurii is given by the series of modulo calculations as follows:

$$F_{SP_1} = \left(\frac{R_1}{N_C}\right) F_0$$

$$F_{SP_2} = \left(\frac{R_2}{N_c}\right) F_0$$

$$F_{SP_n} = \left(\frac{R_n}{N_c}\right) F_0$$

where
$$R_1 = \text{modulo}\left(\frac{N_c}{N_R}\right)$$

$$R_2 = modulo\left(\frac{N_R}{R_1}\right)$$

$$R_3 = \text{modulo} R_1/R_2$$

$$R_n = \text{modulo} \frac{R_{n-2}}{R_{n-1}}$$

B

Z

1

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$$F_{SP}_{n}$$
 = frequency of the n'th spurious frequency, and modulo $\frac{A}{B}$ = A-kB where k = maximum integer A/B

The amplitude of the spurious frequencies (relative to the fundamental frequency amplitude $(A_{\rm S})$ is given by:

$$A_S = Ampl.$$
 of $F_S \approx N_c$ (amplitude of the desired signal)

$$A_{SP_1} \simeq \frac{N_R}{N_C} = \frac{F_S}{F_O}$$

$$A_{SP_2} \simeq \frac{R_1}{N_c} = \frac{F_{SP1}}{F_0}$$

$$A_{SPn} = \frac{R_{n-1}}{N_c} = \frac{F_{SP(n-1)}}{F_o}$$

The above amplitudes are shown as approximations since the sum of the amplitudes of the fundamental and all the spurii must equal l. Thus, if some spurii exist, the fundamental amplitude must be less than $N_{\rm c}$. However, if the total sum of all the spurii amplitudes is much smaller than the fundamental amplitude the above approximations become almost equalities.

An example of the application of the above equations is demonstrated in Table 4-1 for three examples. One example is a relatively clean spectrum which occurs when $N_{\rm c}$ is greater than but approximately equal to an integer multiple of $N_{\mbox{\scriptsize R}}$. Another example is a spectrum richer in higher frequency spurious signals which occurs when N_c is less than but approximately equal to an integer multiple of N_{R} and a third example is very rich in spurious signals resulting when $N_{\ensuremath{\text{c}}}$ is not close to an integer multiple of N_R . The spurious frequencies can be demonstrated to be the result of beat frequencies between a harmonic of the clock frequency (F_0) and a harmonic of the synthesizer frequency (F_s). For example, the 10 Hz spurious, shown in the table, occurs from a beating of the clock frequency with the 10th harmonic of the synthesizer frequency. This beating approach, however, does not put forth a technique to determine which spurii are present and their amplitudes. The technique of calculating residues can be shown to predict every spurious signal and its particular level.

TABLE 4-1: SPECTRA OF SOME ARITHMETIC SYNTHESIZER OUTPUTS

Assumptions $N_c = 1,000,000, F_o = 1 \text{ MHz}$ EXAMPLE #1: $Nr = 99,999, F_s = \frac{99,999}{1,000,000} = \frac{99,999 \text{ kHz}, F_o}{F_s} = 10.0001$

		A _{SPi} (RELATIVE TO A _S)					
R _i	F _{SPi}	Linear Level	dB Level				
$R_1 = 10$	10 Hz	.099999 = 0.1	- 20 dB				
R ₂ = 9	9 Hz	.00001	-100 dB				
$R_3 = 1$ $R_4 = 0$	l Hz D. C.	.000009 .000001	-101 dB -120 dB				

TABLE 4-1: SPECTRA OF SOME ARITHMETIC SYNTHESIZER OUTPUTS (CON!T)

EXAMPLE #2:
$$N_R = 100,001$$
 $F_s = 100.001$ kHz $\frac{F_o}{F_s} = 9.9999$

		A _{SPi} (RELATIVE TO A _S)					
Ri	FSPi	Linear Level	dB Level				
R _{]=99,991}	99.991 kHz	ا. شير 100001.	- 20 dB				
$R_2 = 10$	10 Hz	.0999911	- 20 dB				
$R_3 = 1$	1 Hz	.00001	-100 dB				
$R_4 = 0$	D.C.	.000001	-120 dB				

EXAMPLE #3:
$$N_R = 105,000$$
, $F_s = 105 \text{ kHz}$, $\frac{F_o}{F_s} = 9.524$

Ï		-	A _{SPi} (RELATIVE TO A _S)						
	Ri	F _{SPi}	Linear Level	dB Level					
	$R_1 = 55,000$	55 kHz	.105	-19.6 dB					
	$R_2 = 50,000$	50 kHz	.055	-25.2 dB					
	$R_3 = 5,000$	5 kHz	.050	-26.0 dB					
	$R_4 = 0$	D.C.	.005	-46.0 dB					

A frequency domain plot of these spectra are shown in Figure 4-6, which shows the relative purity of each of the different frequenc-The spectra shown are the output of the D/A converter, before any filtering occurs. If the D/A output signal is a sawtooth waveform, then all spurious signals will also be sawtooth waveforms. Thus, the spurii will contain harmonics that fall off as 1/n2 (in terms of power). It would be desirable if all spurii frequencies could be placed above F_{ς} , since then the fundamental spurii and all harmonics would be further above F, and could be easily rejected by a low pass or band pass filter. However, all residue values must be less than N_p . Since the synthesizer fundamental frequency is (N_R/N_c) and the spurii have a frequency $(R_i/N_c)F_o$, then all spurii are less than F_S . Thus, since all spurii are less than F_S and the spurii harmonics only fall off as $1/n^2$, the optimum (for least spurii energy on the filtered output) synthesizer frequency is one which produces only very low frequency spurii. A narrow band pass filter could be placed on the D/A output signal which would pass only the fundamental frequency (F_s) and very high order harmonics of the spurii. Since these high order harmonics would be of very low level, they would not represent a significant phase jitter on the synthesizer output. For example, if the synthesizer frequency, containing the doppler shift, was not allowed to vary more than, say, a kilohertz, the highest frequency spurious would be about 10 kHz (assuming the nominal parameters of Table 4-1) and its level would be 20 dB below the synthesizer signal. The 10th harmonic of this spurious would be in the bandpass of the synthesizer filter, but it would be reduced by an additional 20 dB. Thus, the highest level spurious signal out of the bandpass filter would be 40 dB below the synthesizer fundamental signal. The effect of these spurious levels on the doppler extraction accuracy depends highly on the type of interface with the S-vand transponder. If the synthesizer frequency is multiplied to the interface frequency, then F_s will only vary a small amount and low spurious levels would result. However, the multiplication process would raise the spurii significantly. If F_s is translated to the interface frequency, then F_s would vary over a

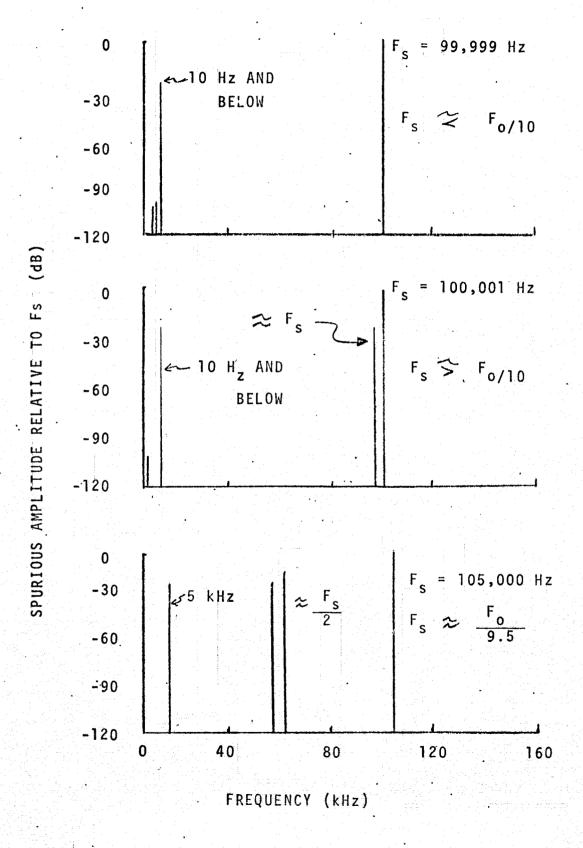


FIGURE 4-6 SPURIOUS LEVELS VERSUS SYNTHESIZER FREQUENCY

larger range, due to the doppler, resulting in higher level spurii at F_S . However, these spurii would not be increased in level when translated to the interface frequency. Thus, a trade-off exists between frequency multiplication and frequency translation in order to obtain the lowest spurii level, and hence the greatest doppler accuracy.

4.2.3.3 S Band Interface Technique for Reduced Spurious Levels

The spurious content present in the first low pass filter (the loop filter immediately following the first phase detector preceding the A/D converter) will determine the accuracy of the extracted doppler. That is:

$$\epsilon_{\text{Fd}} = \frac{R}{2 \text{ TT} \pm \sqrt{(\text{S/N})_{\text{LOOP}}}}$$

K

1

where R is the ratio of counted doppler (in the accumulator).

 $(S/N)_{LOOP}$ = S/N level in the first loop preceding the A/D converter.

With a frequency multiplying loop, the bandpass filter could be made very narrow since the total frequency variation at the D/A output would only be \pm 20 Hz (with K \simeq 100) for the maximum range of doppler off-set. With this narrow a bandpass filter a very large percentage of the spurious harmonics would be rejected. However, a bandpass filter centered on about 500 KHz to 1 MHz and with only 40 Hz bandwidth is not practical. Furthermore, any spurii that would be present would be increased in amplitude due to the frequency multiplication value (K).

The doppler error resulting from the spurious levels can be minimized by either minimizing R or maximizing the loop S/N level. R would be minimized if the DVCO frequency is translated to the S band interface frequency, since R=27.625K and K=1 (a minimum) for the translation technique. The translation technique also reduces the spurious level, and hence the loop S/N ratio, since the spurious signals are not multiplied by large values of K.

In the translation technique, the D/A output carries the full doppler frequency off-set that is present on the interface frequency (\pm 2500 Hz on a 76.083 MHz interface). Thus, the bandpass filter would need to have a bandwidth of 5 kHz to pass the full doppler range. The high level spurious frequency could be as high as 50 kHz for the translation technique (if the synthesizer output frequency is approximately 500 kHz). Thus, the 10th harmonic of this spurious would be present in the output of the bandpass filter. With a sawtooth output on the D/A converter, the spurious would only be reduced an additional 20 dB. The resultant S/N ratio would be 40 dB (-20 dB spurious reduced by an additional 20 dB). As will be shown later, the D/A converter could produce a triangular waveform and the spurious would be reduced by 40 dB, resulting in a S/N level of 60 dB at the bandpass filter output. Since the translation technique would not increase the noise level, the S/N ratio in the first loop filter would be no lower than 60 dB. Actually, the low pass filters in the phase lock loop could be made smaller than the 5 kHz bandwidth of the D/A output filter. Thus, the S/N level could be much higher than 60 dB, if the spurious signals fell outside the loop response. For example, a 500 Hz loop bandwidth could reduce the total noise contribution from all spurii by an additional 10 dB, resulting in a S/N ratio of 70 dB in the first low pass loop filter.

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SECTION 5

SYSTEM DEFINITION AND TRADE-OFFS

5.1 SELECTION CRITERIA

This section defines a doppler extraction system using the arithmetic synthesizer as a digitally controlled VCO. To define this system in further detail requires a trade-off of the transponder interface technique (that is, DVCO frequency multiplication versus frequency translation) and the related definition of loop bandwidths, DVCO frequency and register capacities in the arithmetic synthesizer. The prime concern in the selection and design of the DVCO is the resultant total doppler error. Other factors are also important for a flight hardware design of a doppler extractor. These include cost, power consumption, weight, volume, circuit complexity and reliability. While these parameters do not vary significantly, they do affect the total error budget.

For example, in the selection of frequency multiplication, or frequency translation, there is little advantage of one system over the other in terms of cost, power consumption, weight, etc. Frequency multiplication requires the addition of a frequency multiplying VCO loop, whereas frequency translation requires substitution of the multiplying loop with a fixed injection oscillator or phase lock-loop. Both of these techniques therefore require approximately the same amount of hardware. However, because the error sources are affected significantly, the system trade-offs and optimizations have primarily concentrated on minimizing the total error budget.

5.2 SYSTEM SELECTION

The error analysis has shown that only the quantization error and noise induced jitter errors are sensitive to the S-band transponder interface techniques. The quantization error is directly proportional to R, the ratio of S-Band doppler to arithmetic synthesizer doppler. Thus, in multiplying the synthesizer frequency directly to the interface frequency, the quantization

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error is multiplied by the same amount. Translation of the synthesizer frequency does not multiply the error and is thus preferred for minimum quantization error.

However, the quantization error can be made arbitrarily small by choosing the register and accumulator capacities sufficiently large. Thus, either interface technique can result in a very low quantization error, although frequency multiplication would require about 6 more bits in each of the frequency and accumulator registers.

The jitter error, caused by internal DVCO noise (from spurious signals and D/A conversion noise), is higher when the DVCO frequency is multiplied rather than translated. Section 4 has shown that the internal noise induced jitter results in an S-Band doppler error given by

$$\sigma_{FD} = \frac{R}{2\pi t \sqrt{(S/N) \log p}}$$

With frequency multiplication, R has a value of F_s BAND/ F_{ARITH} SYNTH, which is at least 2000 for a synthesizer frequency of 1 MHz or less. Thus, to achieve 0.01 Hz or less of jitter error, the loop S/N ratio would need to be at least 90 dB.

This S/N level could possibly be achieved but only at the expense of designing a very narrow band pass filter on the D/A output and by maintaining the synthesizer frequency very close to a integer ratio of the clock frequency. For example, if a sawtooth waveform is generated at the D/A output and the pre-filtered spurious signals are only 20 dB below the fundamental signal, then the D/A bandpass filter must supply an additional 70 dB of spurious rejection.

Even with a 1 MHz synthesizer frequency, the highest frequency spurious signal must be $1/\sqrt{10^7}$ of the synthesizer frequency (3100th harmonic = 1 MHz), or 300 Hz. The filter bandwidth would also need to be in the order of 300 Hz to prevent several spurious signals from occurring in the filter bandpass. This results from the fact that the spurious harmonics are spaced in 300 Hz increments.

The loop bandwidth must be further reduced to eliminate the noise caused by D/A conversion noise. With a 10 bit D/A converter, and a clock frequency as high as 10 MHz, the overall loop bandwidth must be $1.8~\mathrm{Hz}$ (with K = 76 and a synthesizer frequency of 1 MHz). The use of a 12 bit D/A converter would only increase the bandwidth requirement to about 7 Hz. These bandwidths are not desirable for acquisition and high accuracy tracking.

The frequency translation technique can relax these requirements significantly. In the equation for noise induced jitter, R has a fixed value of 27.625 (for the 76 MHz transponder interface). The S/N required for a 0.01 Hz doppler error (at S-band) then becomes only 53 dB.

The spurious frequencies, however, could be as high as 100 kHz with a 1 MHz synthesizer frequency and a 10 MHz clock. Thus, only the 10th harmonic of the spurious will fall in the D/A filter pass band. With a sawtooth waveform on the D/A output, the 10th harmonic of the spurious would be only 40 dB below the fundamental synthesizer frequency. As will be shown, the use of a triangular wave could reduce the spurious levels to -60 dB, with a resultant S/N ratio of +60 dB. Further, the bandpass filter could have a bandwidth approaching 50 kHz without increasing the noise due to multiple spurii at the filter output.

The D/A conversion noise is also reduced to insignificant levels. Based on paragraph 4.2.3.1, a S/N ratio of 100 dB can be achieved with a net loop bandwidth of 500 Hz.

Thus, the translation technique is a preferred alternative to frequency multiplication and is the technique recommended for a high accuracy one way doppler extractor.

5.3 PERFORMANCE OPTIMIZATION

As the analysis has shown, the quantization error can be made arbitrarily small. The oscillator error can be minimized by using very stable oscillators, if the size and cost are not objectionable.

The external signal-to-noise ratio is more than adequate for a typical loop bandwidth (similar to the receiver loop bandwidth). The

noise and spurious signals generated as part of the arithmetic process. The following techniques can reduce this source of doppler error below the desired 0.01 Hz accuracy at S-Band. There are undoubtedly other spurious reduction: techniques, which may be found as part of further study during a hardware implementation program.

5.3.1 SYNTHESIZER AND CLOCK FREQUENCY SELECTION

The spurious signal amplitudes can be made lower by selecting a synthesizer frequency, which is much lower than the clock frequency. Recalling that the highest amplitude spurious, and also the highest frequency spurious has a frequency and amplitude given by:

$$F_{SP \text{ max}} = \frac{R_1}{N_c} F_0$$

$$A_{SP \text{ max}} = \frac{N_R}{N_c} = \frac{F_s}{F_0} \text{ volts}$$

$$A_{SP \text{ max}} = \frac{N_R^2/N_c^2}{F_0^2} = \frac{F_s^2}{F_0^2} \text{ in power}$$

Thus the magnitude of the highest level spurious is decreased in power by the square of (N_R/N_c) or by the square of (F_S/F_o) , since the synthesizer frequency is $[F_S=(N_R/N_c)\ F_o]$. A reduction of this frequency to 1/10th its former value would reduce the spurious levels by 20 dB. Alternatively, if the clock frequency is increased 10 fold, and F_S is held constant, the spurious levels are also decreased in amplitude by 20 dB. Thus, the synthesizer clock frequency should be chosen as high as the digital logic will permit, provided other factors, such as power consumption, do not become prohibitive.

Figure 5-1 shows the sensitivity of the maximum spurious level to

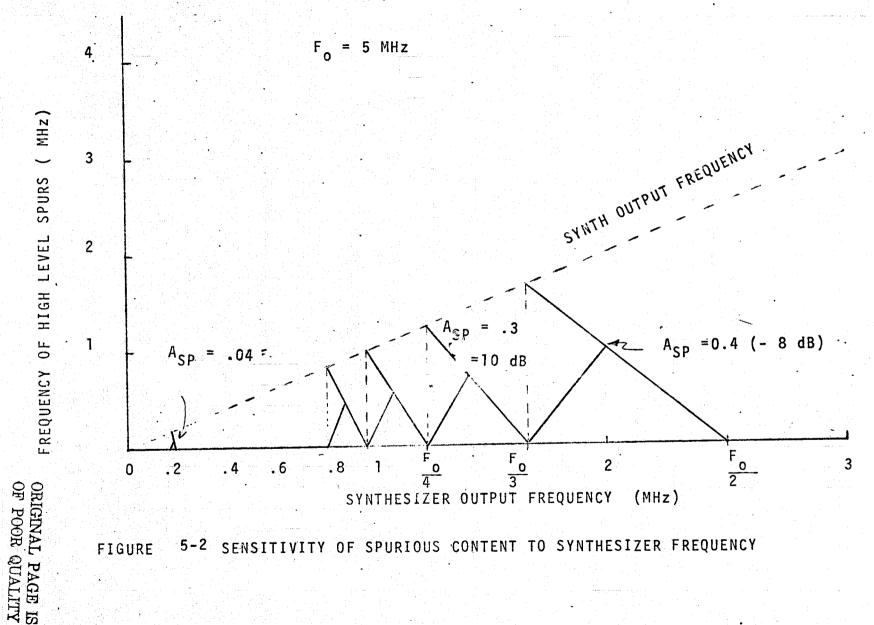
FIGURE 5-1 SENSITIVITY OF SPURIOUS AMPLITUDE TO SYNTHESIZER FREQUENCY

the ratio of synthesizer to clock frequency. The results show that very low spurious levels can be achieved (<-60 dB for example) if the synthesizer frequency is a small fraction of the clock frequency ($10^{-3}F_0$ or less). However, if the synthesizer frequency must be kept high, to carry a large doppler off-set, for example, then a value of F_s/F_0 less than 10^{-3} may only be achieved by choosing a very high clock frequency. This would require high speed logic circuits in the arithmetic circuits.

The frequencies of the high level spurii are shown in the curves of Figures 5-2 and 5-3 for a clock frequency of 5 MHz. These curves show the high and low frequency spurii that exist when F_s is slightly greater than an integer fraction of the clock frequency. The curves also show the lack of any spurii for synthesizer frequencies at exact integer ratios of the clock, and only a very low frequency spurious when F_s is slightly lower than an integer fraction of the clock frequency. Since all other spurious signals that might be present on the D/A output are lower in both frequency and amplitude than the ones shown in the figures, the curves represent a worst case envelope for the spurious content.

The level of the spurii shown in Figure 5-3 are approximately 20 dB below the synthesizer outputs. If the interface frequency is translated, the doppler variation on ${\sf F}_{\sf S}$ would be the same as at the 76 MHz interface, namely \pm 2.5 kHz. Thus, if ${\sf F}_{\sf S}$ is chosen slightly more than 5 kHz below 500 kHz (${\sf F}_{\sf O}/10$) only one low frequency (but high level) spurious will occur. The maximum frequency of this spurious would be 50 kHz (as shown in Figure 5-3) and the 10th harmonic would fall in the synthesizer band pass filter response. Thus, after the filter output the spurious would be reduced to -40 dB relative to ${\sf F}_{\sf S}$.

A spurious level of -40 dB would result in a doppler extraction error of 0.04 Hz. To reduce this error to 0.01 Hz (-53 dB) would require either increasing the clock frequency by four to 20 MHz, reducing the synthesizer frequency to 125 kHz, or generating triangular instead of sawtooth waveforms at the D/A output. Any one or combination of these techniques could be used to reduce the spurii amplitude.



SENSITIVITY OF SPURIOUS CONTENT TO SYNTHESIZER FREQUENCY FIGURE

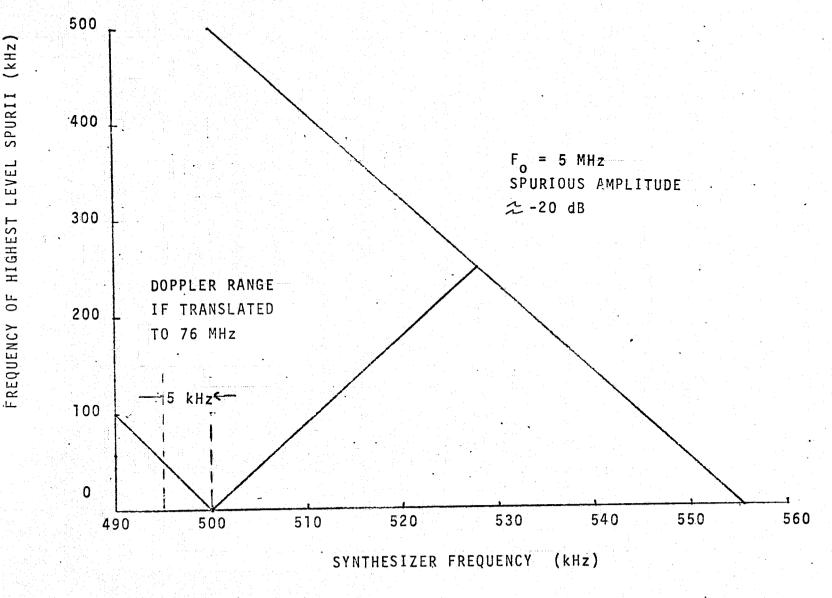


FIGURE 5-3 SPURIOUS FREQUENCIES AROUND F₀/10

5.3.2 SYNTHESIZER WAVEFORM FOR LOW SPURIOUS LEVELS

The baseline DVCO uses the arithmetic synthesizer with a D/A converter directly connected to the accumulator output. With this technique, the D/A converter output is a sawtooth voltage. However, it is possible to add complementing logic to the accumulator output before transfer to the D/A converter. The resultant D/A output would be a bi-polar triangular waveform as shown in the diagram of Figure 5-4.

Also shown in the figure are the accumulator outputs and the required complementing logic for each quadrant of the signal. With this technique the synthesizer output frequency and amplitude is given by:

$$F_s = \frac{N_R}{4 N_C} F_0$$

$$A_s = + N_c = 2 N_c$$
 (Peak to Peak)

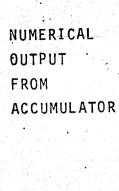
Notice that for the same register number and accumulator capacity, the frequency is 1/4 the previous value (for the sawtooth waveform) and the amplitude is twice as large. The amplitude shown above, by itself means very little since the actual amplitude of the D/A output can be any desirable value determined by the D/A drive voltage. However, with the aid of Figure 5-1, the amplitude of the spurii follow the same relationships as presented earlier, except that $\rm H_{\rm C}$ is replaced by 4 $\rm H_{\rm C}$. That is:

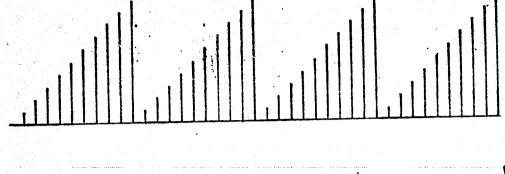
$$R_{1} = \text{modulo} \frac{4N_{c}}{N_{R}}$$

$$R_{2} = \text{modulo} \frac{N_{R}}{N_{R}}$$

$$R_{3} = \text{modulo} \frac{R_{1}}{R_{2}}$$

$$R_{n} = \text{modulo} \frac{R_{n-1}}{R_{n-2}}$$





QUADRANT LOGIC POSITIVE COMPLEMENT NEGATIVE
OF NUMBER OF NUMBER

NEG. COMP. OF NUMBER

OUTPUT OF D/A CONV.

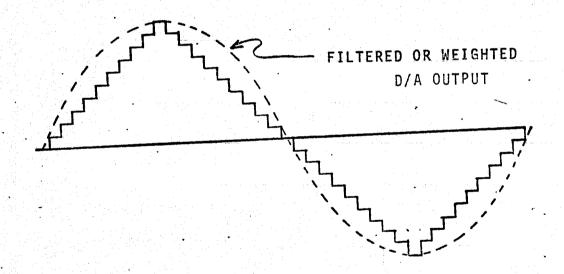


FIGURE 5-4 SYNTHESIZER WAVEFORM WITH QUADRANT LOGIC

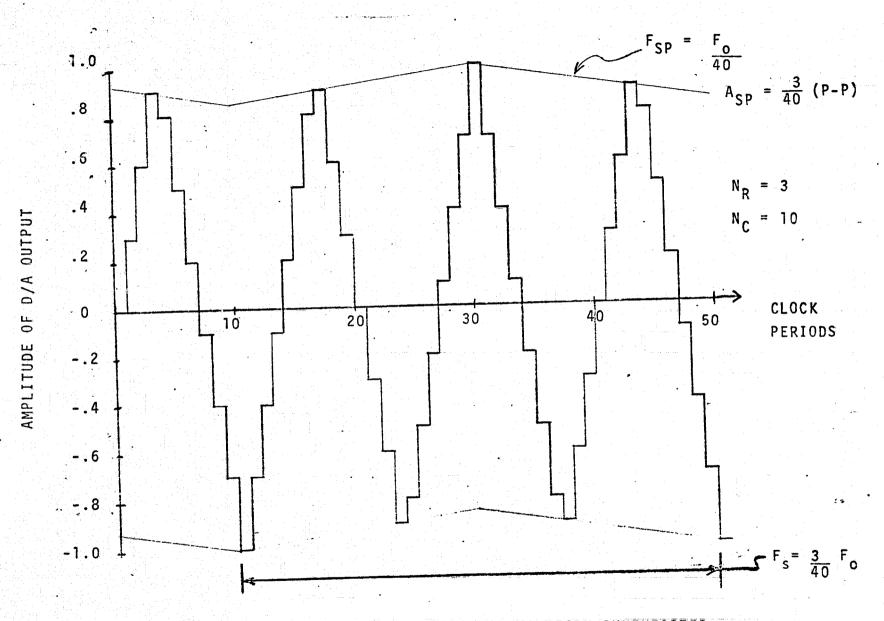


FIGURE 5-5 SPURIOUS SIGNALS FOR TRIANGULAR WAVEFORM SYNTHESIZER

Relative to the fundamental output, the spurii have frequencies and amplitudes given by:

$$F_{SPN} = \frac{R_{n}}{4 N_{c}} F_{0}$$

$$A_{SP1} = \frac{+ N_{R}/4}{N_{c}} = \frac{N_{R}}{4 N_{c}} = \frac{F_{s}}{F_{0}} \text{ (Peak to Peak)}$$

$$A_{SPN} = + \frac{R_{n}(1/4)}{N_{c}} = \frac{R_{n-1}}{4 N_{c}} = \frac{F_{SP(n-1)}}{F_{0}} \text{ (Peak to Peak)}$$

In comparing the above equations with the equations for the sawtooth waveform, the spurii frequencies are identically the same, if the residue values are the same. For the same output frequency and the same register number, the value 4 $\rm N_{\rm C}$ for the triangular wave would be identically equal to the value $\rm N_{\rm C}$ for the sawtooth wave. Thus, the residue values would be identically the same and all spurious frequencies and amplitudes would be the same. However, as shown in Figure 5-5, the triangular output generates spurii with triangular waveforms, whereas the sawtooth output generated spurii with sawtooth waveforms.

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There is a significant difference when only high order harmonics of the spurii are present in the filtered output. The harmonics of a sawtooth waveform fall off as $1/n^2$ (in power), whereas the harmonics of a triangular wave fall off as $1/n^4$. Thus, if the 11th harmonic of a triangular waveform spurious is in the pass band of the D/A output filter, then the spurious harmonic would be 41.7 dB lower then the fundamental spurious. For a comparable sawtooth spurious, the harmonic would only be 20.8 dB below the fundamental spurious amplitude. Thus, a significant advantage may be achieved in spurious reduction by using triangular waves where harmonics of spurii are expected to fall in the DVCO output passband. Furthermore, there are no even harmonics for a truly triangular waveform.

5.4 SYSTEM DEFINITION

The recommended technique for interfacing the DVCO with the transponder doppler reference frequency is to translate the transponder output frequency down to the DVCO frequency.

5.4.1 BREADBOARD CONFIGURATION

A block diagram of the recommended breadboard doppler extraction system, interfacing at the 76 MHz interface frequency of the Apollo USB transponder is shown in Figure 5-6. The 76.083 MHz transponder output is translated to a 1.083 MHz signal by means of the 75 MHz fixed injection oscillator. The 1.083 MHz output contains a fraction of the original doppler signal.

The DVCO loop senses the phase error between the DVCO frequency and the 1.083 MHz reference, and converts this error to an incremental change ($ightharpoonup N_{
m p}$) in the frequency register number. The accumulator generates the linearly increasing numerical values which are converted to an analog waveform by the action of the D/A converter. The bandpass filter reduces the spurious signals, the D/A staircase levels and the D/A noise. The bandpass filter could be tuned to a harmonic to provide a small amount of frequency multiplication (K=1 or a small integer value) to supply the phase detector with a 1.083 MHz DVCO frequency. By choosing the synthesizer clock frequency close to an integer multiple of the output frequency, the amplitude of the filtered spurious signals is minimized. If K had a value of 1, the synthesizer frequency would be 1.083 MHz, which is almost half way between Fo/4 = 1.25 MHz and Fo/5 = 1.00 MHz. However, if K had a value of 2, the synthesizer frequency would be 541.667 kHz which is about 14 kHz below Fo/9 =555.556 kHz. Thus, a value of 2 for K allows the synthesizer frequency to be chosen near a sub harmonic of the clock frequency for low spurious levels.

5.4.2 FLIGHT HARDWARE CONFIGURATION

A configuration that could operate from any of four S-band frequencies is derived from the flight hardware design of Volume 1 and is shown in Figure 5-7. The Space Shuttle clock frequency is specified at Fo = 4.608 MHz, while typical S-band receiver interface

Figure 5-6. Recommended Breadboard Doppler Extractor

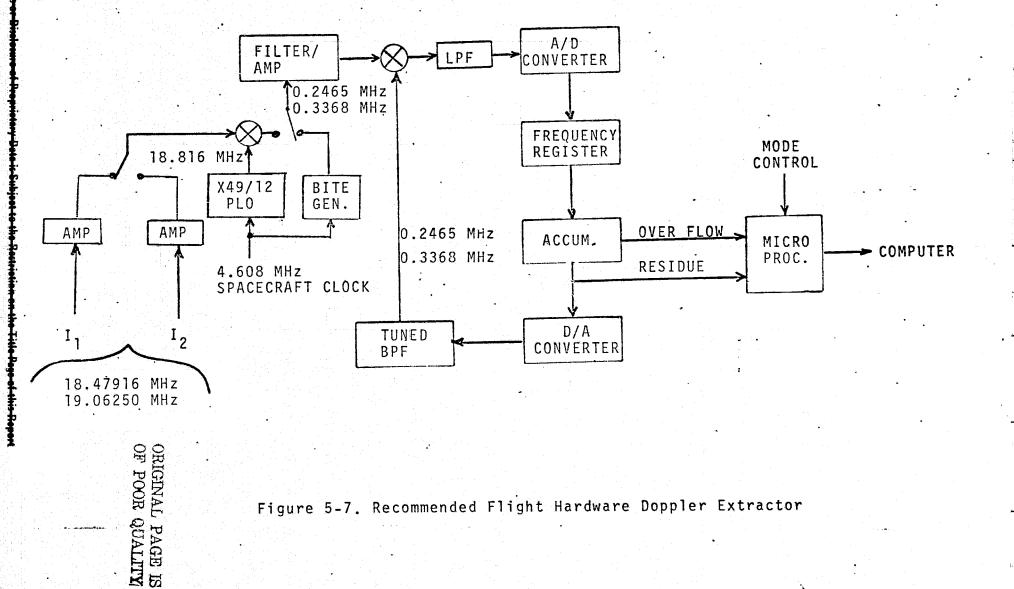


Figure 5-7. Recommended Flight Hardware Doppler Extractor

frequencies are 18.4791667 MHz and 19.0625 MHz. The previously selected offset frequency of $\frac{49}{12}$ x 4.608 MHz = 18.816 MHz would result in doppler reference frequencies of 336.833 kHz and 246.5 kHz respectively. Locking to these frequencies is definitely within the capabilities of the arithmetic synthesizer DVC0

Alternately an even simpler offset frequency of 4x4.608 MHz = 18.432 MHz may be considered. The resulting difference frequencies would then be 39.667 kHz, and 630 kHz, respectively. Again the DVCO can lock directly to these frequencies or a low order harmonic may be used if this proves advantageous. The exact choice would be made when the S-band transponder for the Space Shuttle is further definitized and all interface frequencies are firmly specified by the selected contractor.

5.5 IMPLEMENTATION CONSIDERATIONS

The DVCO doppler extractor consists of three functional units, namely the frequency translator, the DVCO and the digital processor. The frequency translator used in a breadboard, with the Apollo USB transponder at the 76.083 MHz interface, would be the same as the 75 MHz injection oscillator/mixer used in the vernier breadboard described in Volume 1. The digital processing functions of time interval counting, doppler cycle counting, fractional cycle computation, display and computer formatting as well as display parameter computation would be performed by a microprocessor with a minimum of dedicated hardware circuits. Use of a more powerful microprocessor than the one described in Volume 1 will result in a significant reduction of the amount of dedicated hardware and a net reduction in the overall package count.

Digital technology continues to improve, and microprocessor techniques have developed to the point where the use of a general-purpose microprocessor is practical for the processing of all the doppler extractor data. It is proposed that all of the processing, mode control, and computer interface functions be performed by a microprocessor. A bit-slice unit, expandable to a 32-bit word

length is preferred. This approach would result in a substantial reduction in the hardware package count, at the expense of increased software complexity. For example, performing the binary-to-BCD conversion of the extractor data in the microprocessor software would eliminate fully half of the counter and latch stages required in the existing vernier technique breadboard.

With the development of improved compilers and assemblers for the new microprocessors, the software design should become increasingly simpler. Thus in the long run this approach will become more practical for use in the extractor, as well as other spacecraft navigation equipment functions.

The arithmetic synthesizer (DVCO) is currently being developed by RCA in LSI form under Air Force Contract F33615-74-C-1123. All digital logic including the frequency register, the phase register, and the adder are being placed on a single LSI array in units of 8 stages. Three chips would thus constitute a 24 stage arithmetic synthesizer. The design uses silicon gate double epitaxial CMOS/SOS technology to allow operation at clock frequencies up to 20 MHz at relatively low power dissipation. The projected array size is 214 mils x 178 mils and it will contain about 1060 devices. The array is similar in density to previously processed 8 bit x 8 bit multiplier arrays which have exhibited good yield characteristics during processing and test.

APPENDIX A

United States Patent

Butler

(15) 3,689,914

[45] Sept. 5, 1972

[54] WAVEFORM GENERATOR[72] Inventor: Jaquith Gould Butler, Cherry Hill,

N.J.

[73] Assignce: RCA Corporation,

[22] Filed:

Aug. 9, 1971

[21] Appl. No.: 170,296

Related U.S. Application Data

[63] Continuation of Ser, No. 836,751, June 26, 1969, abandoned.

[52] U.S. Cl.340/347 DA, 235/197, 328/14, 328/181, 328/185, 235/175

[58] Field of Search ...307/227, 228; 325/38; 328/13, 328/14, 181, 185, 186; 235/197, 150.53, 175; 340/347 DA

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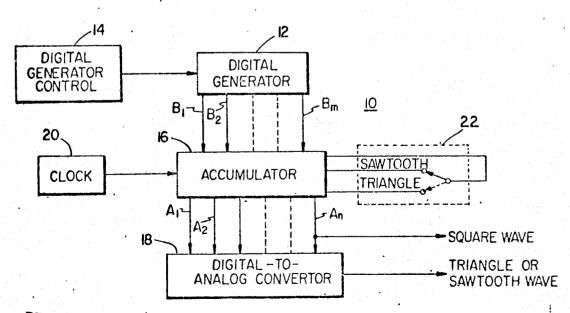
3,337,863	8/1967	Lender325/38
3,349,195	10/1967	Gray340/347 X
3,490,049	1/1970	Choquet et al340/347 X

Primary Examiner—Thomas A. Robinson
Assistant Examiner—Charles D. Miller
Attorney—Edward J. Norton

[57] ABSTRACT

A waveform generator is disclosed in which a constant binary signal is applied to a digital accumulator. For every clock pulse, the accumulator adds the binary signal and its stored contents and then stores the added sum. Periodically the accumulator becomes full and at the next clock pulse, the value of the contents returns to approximately zero. The stored signal from the accumulator is applied to a digital-to-analog converter and an analog signal is derived therefrom corresponding to the binary number stored in the accumulator. A periodic wave appears at the output of the digital-to-analog converter having a frequency equal to $K/2N \times f_c$ where K is the analog value of the constant, N the number of stages in the accumulator, and f_c the clock frequency. This frequency can be varied within one clock cycle without causing a phase discontinuity in the output signal by merely changing the value of the constant binary signal.

5 Claims, 9 Drawing Figures





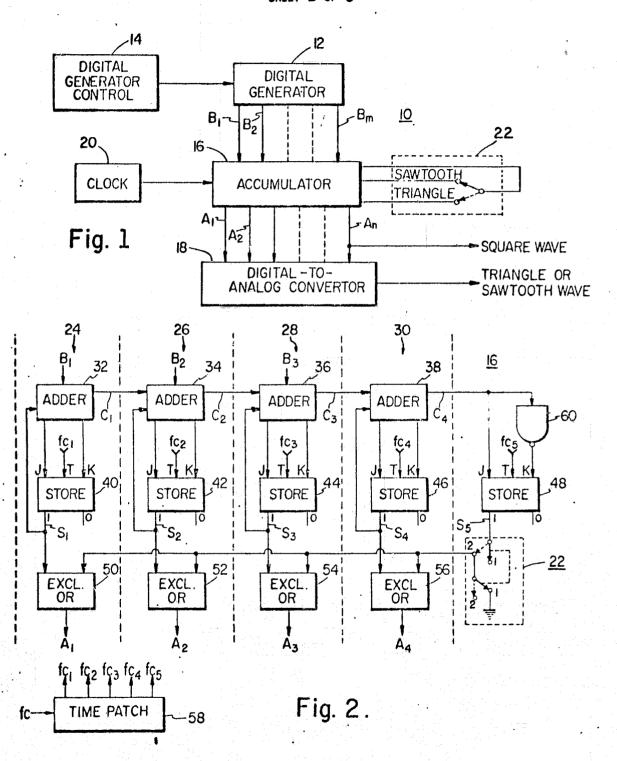
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SHEET 1 OF 5



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SHEET 2 OF 5

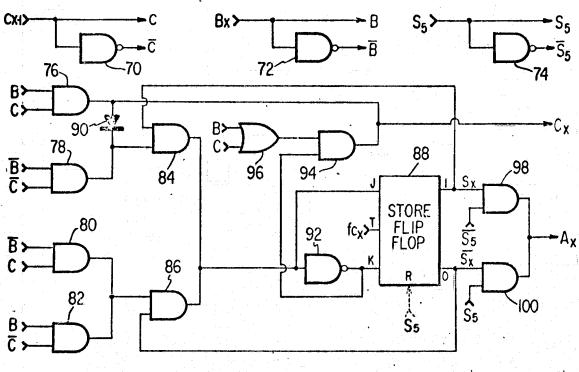


Fig. 3.

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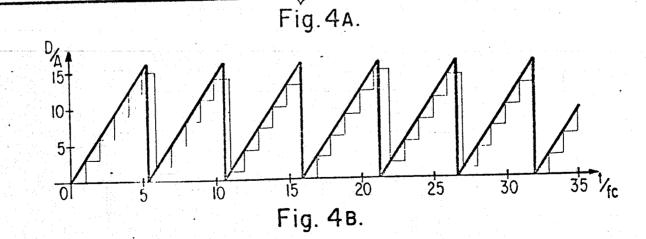
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Accumulator

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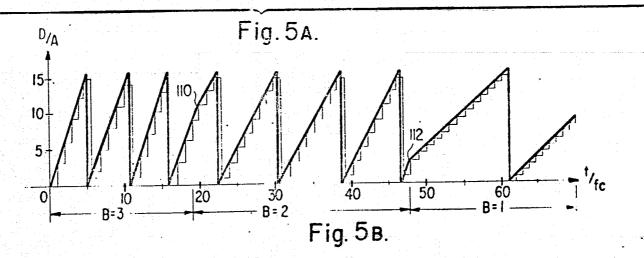
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21	0	1	0	1	0	1	1	13	
22	0	1	0	1	1		1	15	
23	0	1	0	1	0	0	0	1	
24	0	1	0	1	1	0	0	3	
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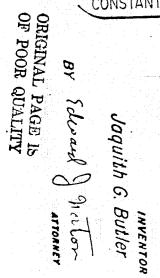
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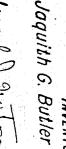


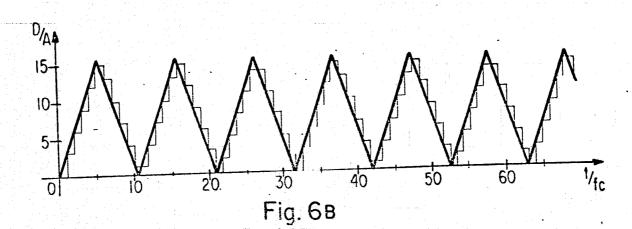
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Fig. 6A.







WAVEFORM GENERATOR

This is a continuation of my copending application, Ser. No. 836,751, filed June 26, 1969 and now abandoned.

This invention relates to waveform generation and 5 more particularly to apparatus for generating a constant frequency waveform in which the frequency may be changed within one cycle.

In existing frequency synthesizers or other types of waveform generators, a major problem is changing the 10 frequency of the waveform during the operation of the equipment with which the generator is associated. When it is desired to change the frequency of the voltage controlled oscillator of a typical digital frequency synthesizer, the divisor of a variable dividing network is 15 changed causing an imbalance in the phase lock loop. A phase comparator then changes the control voltage applied to the oscillator causing it to oscillate at a different frequency. Eventually the loop again becomes phase locked and a constant frequency is attained. 20 However, it takes a considerable time to relock the loop and during this time the oscillator is oscillating at many different frequencies none of which are desired. One serious consequence of this is that during the lockup time, it is impossible to properly operate the equip- 25 ment to which the oscillations are applied due to the fact that the undesirable frequencies are occurring.

The above problem is clearly perceived when for instance, it is desired to use a frequency to control the speed of a motor. If it is desired to reduce the speed by 10 percent, a mere change of the dividing network in the phase lock loop type frequency synthesizer will eventually do this but in the mean time the synthesizer will be at frequencies quite a bit or higher or quite a bit lower than either the desired or the initial frequency. Thus the motor will be speeding up and slowing down during this time, and generally, this can not be tolerated. Ideally one wishes to be able to change the frequency instantaneously or at least within one cycle so that at one instant the old frequency is occurring and the next instant the new frequency is occurring.

In another type of frequency synthesizer it is possible to change frequencies by switching different crystals into and out of the oscillator circuit, but again this type of synthesizer produces large phase and amplitude transients when the switching occurs.

It is an object of this invention to provide an improved variable frequency waveform generator.

There is provided means for generating a digital signal which is applied to an accumulator. The accumulator accumulates and stores a digital signal and the output of the accumulator is applied to a digital-to-analog converter which reads the stored contents of the accumulator in analog form. The accumulator generates a wave having a frequency which is determined by the digital signal applied to the accumulator.

The invention is better understood with reference to the drawing in which:

FIG. 1 is a block diagram of a waveform generator according to one embodiment of the invention;

FIG. 2 is a block diagram of the accumulator shown in FIG. 1;

FIG. 3 is a diagram of one stage of the accumulator shown in FIG. 2; and

FIGS. 4 through 6 are digital tables and corresponding waveforms useful in describing the operation of the invention.

Referring now to FIG. 1, variable frequency waveform generator 10 includes a digital generator 12 and a digital generator control 14, digital accumulator 16, digital-to-analog convertor 18, and clock 20.

Digital generator 12 and digital generator control 14 act together to produce a desired digital number in binary form of M digits at a plurality of outputs $B_1 - B_m$ thereof. There is included in generator 12 a series of gates which are responsive to digital generator control 14 such that by a mere change of the setting of control 14, generator 12 will provide a different binary signal at its outputs. The least significant digit of the number appears at output B_1 and the most significant digit of the number appears at output B_m . Thus, if a digital number corresponding to "2" were desired, output B_2 would be in the "1" state and outputs B_1 , and $B_2 - B_m$ would be in the "0" state, since the binary number 0-1-0-0...0 corresponds to the number "2".

Accumulator 16 is a digital accumulator which at every clock pulse f_c from clock 20 adds the value of the binary number applied thereto to a number already stored therein and replaces the stored number with the sum. In waveform generator 10, accumulator 16 is an N. stage accumulator where N > M. Each of the first M stages of accumulator 16 has a corresponding one of the outputs $B_1 - B_m$ of digital generator 12 applied to it. Thus, the B₁ output from digital generator 12 is applied to the first stage the B2 output to the second stage and so forth. Accumulator 16 has a plurality of outputs, A1 -A_n, each of which is an output of a corresponding stage, and each of which will have a "1" or a "0" thereat. The outputs $A_1 - A_n$ of accumulator 16 are coupled to digital-to-analog converter 18 which converts the then existing stored binary number appearing at these outputs into an analog voltage.

Waveform generator 10 is arranged so that three different types of frequency varying waves can be obtained therefrom. By taking the signal from the final stage output A_n of accumulator 16, a square wave may be obtained and the digital-to-analog 18 converter would be unnecessary. On the other hand, by including digital-to-analog converter 18 in the system and taking the output signal therefrom, either a sawtooth wave or a triangle wave may be obtained, depending upon the position of switch 22. If switch 22 is set at the "sawtooth" position a sawtooth wave appears at the output of digital-to-analog converter 18 and if switch 22 is set in the "triangle" position, a triangle wave will appear at the output of digital-to-analog converter 18. The implementation of this feature is explained hereinafter.

Referring now to FIC. 2, a more detailed diagram of a four N stage 24, 26, 28 and 30 accumulator 16 is shown where M is equal to three. In accumulator 16, there is an adder circuit 32, 34, 36 and 38, a store circuit 40, 42, 44 and 46 and an exclusive OR gate 50, 52, 54, and 56 for each stage and also an overflow store circuit 48. There is also provided a time patch 58.

Each of the store circuits 40-48 is a conventional flip-flop operating in the J-K mode with two control inputs J and K, a trigger input T, and two outputs, "1" and "0". The signal at the "1" output of each store circuit 40-48 will be designated as the S_x signal where x corresponds to the stage of the accumulator in question. Thus the S_1 signal is the signal appearing at the output of store circuit 40 in stage 24.

Each of the adder circuits 32-38 is what is commonly known as a full adder or in other words, a set of logic gates which adds at least two binary numbers and provides signals at a sum output and a carry output. A detailed description of the logic circuit of any one of the adder circuits 32-38 is given in connection with FIG. 3 hereinafter. Each adder circuit has three inputs and three outputs. A respective one of the B_r signals from digital generator 12 is applied to a first one of the inputs of each adder. If there is no corresponding B signal for the adder in question (such as adder 38) it will be assumed that the signal at that input is always "0". Two of the three outputs from each adder are coupled respectively to the J and K inputs of the corresponding store circuits 40-46. These two outputs will always have opposite polarity signal appearing thereat. The third output of each adder circuit 32-38 is the carry output and is applied to the second input of the next stage adder circuit if any, as the carry input signal. 20 As used herein, the signal appearing at the carry output of each adder circuit 32-38 is designated as the C_x signal where x refers to the particular stage with which the adder is associated. Thus, the C_{x-1} signal will be applied to the carry input of each adder circuit. It should 25 diagram of one stage of accumulator 16 which perbe noted that the first stage 24 adder circuit 32 has no carry input signal applied thereto. The C₄ signal from the carry output of the forth stage 30 is applied directly to the J input of store circuit 48 and through invertor 60 to the K input of store circuit 43. The S signal at the "1" output of each store circuit 40-46 is applied as the third and final input to its corresponding adder circuit

The S₁ - S₄ signals are applied to a first input of a corresponding exclusive OR gate 50-56. The S₅ signal is applied to switch 22 which includes two switching arms 62 and 64 each of which may be in either of two positions, 1 or 2. When the switching arms 62 and 64 are in position 1, which corresponds to sawtooth position of switch 22 in FIG. 1, the second input to each of the exclusive OR gates 50-56 will be at ground potential, or in the "0" state. If the switching arms 62 and 64 of switch 22 are changed to position 2, as shown by the dotted line in FIG. 2, a triangle wave can be obtained. In this situation the S₅ signal is applied to the second input of each of the exclusive OR gates 50-56. Timing patch 58 is responsive to the clock signal fe and provides five output signals designated $f_{c}f_{c2}$, f_{c3} , f_{c4} and f_{c5} each of which has the same frequency as the f_c signal.

Accumulator 16, as shown in FIG. 2, operates in the following manner. Each of the adder circuits 32-38 will add the binary value the B, C, and S signals applied to it and apply either a "1" or a "0" to the output coupled to the J input of the corresponding store circuit, a "0" 55 or a"1" to the output coupled to the K input of the corresponding store circuit, and a "1" or a "0" to the carry output, instance if the B, C, and S signal applied to adder circuit 34 are all "1", a "1" will be applied to the J input and a "0" to the K input of store circuit 42, and a "1" signal will appear at the carry output from the adder 34. If two of the three signals are "1", a "0" will be applied to the J input, a "1" to the "K" input, and a "1" to the carry output; if only one of the signals is "1", a "1" will be applied to the J input, a "0" to the K input, and a "0" to the carry output; and finally if all three of the signals are "0", a "0" will be applied to the

J input a "1" to the K input, and a "0" to the carry output. If a "1" is applied to the J input and "0" to the K input of any particular one of the store circuits, the occurrence of a pulse at the trigger input, which is being applied from time patch 58, will cause the "1" output, or the Sx signal, to go to the "1" state if it is not already there. On the other hand if the J input is "0" and the K input is "1", the occurrence of the trigger pulse will cause the "1" output, or the Sx signal, to then go to the "0" state if it is not already there.

The "I" output of each store circuit 40-48 is applied to one input of corresponding exclusive OR gate 50-56. The second input of the exclusive OR gates 50-56 are coupled to switch 22 and will have a "1" or "0" applied thereto. A respective one of the A₁ - A₄ accumulator output signals is taken from the output of each exclusive OR gate 50-56, and its value is determined by the signals applied to the two inputs of that gate. Thus, if the two inputs are the same, that is, both "0" or both "1", the corresponding A. signal will be "0". On the other hand, if the two inputs are opposite, the Az signal will be "1".

Reference is now made to FIG. 3 in which a detailed forms the operations just described is shown. The carry signal from the previous stage is designated C_{x-1} and is applied to invertor 70. In FIG. 3, the C signal is the C_{x-1} signal and the output of invertor 70 is the C signal. A B. signal from the corresponding stage of digital generator 12 is applied to invertor 72. In FIG. 3, the B signal is the B_x signal and the B signal is the signal at the output of invertor 72. Similarly, the S₅ signal is applied to invertor 74 and a signal designated as the S₅ signal a ppears at the output thereof.

Six two-input AND gates 76, 78, 80, 82, 84 and 86 are provided for deriving the signal to be applied to the J and K inputs of store flip-flop 88. The B and C signals are applied to the inputs of AND gate 76 and the B and C signals are applied to the inputs of AND gates ?8. The B and C signals are applied to the inputs of AND gates 80 and B and C signals are applied to the inputs of AND gates 82. The outputs of AND gate 76 is coupled to the anode of diode 90 and the cathode of diode 90 is coupled to the output of AND gate 78 and one input of AND gate 84. The outputs of AnD gates 80 and 82 are coupled together and to one input of AND gate &6. The second input of AND gate 84 is coupled to the "1" output of store flip flop 88 at which appears the \$\overline{S}_{\tau}\$ signal and the second input of AND gate 86 is coupled to the "0" output of store Hip-flop 88 at which appears the S. signal. The outputs of AND gates 84 and 86 are coupled together and applied directly to the J input of store flip-flop 63 and through invertor 92 to the K input of store flip-flop 83.

The output of inventor 92 is also coupled to one input of AND gate 94. The B and C signals are applied to two input OR gate 96, the output of which is coupled to the other input of AND gate 94. The output of AND gate 94 is coupled to the junction of AND gate 76 and the anode of diode 90 and the output carry signal C. for that stage appears at that coupling. The trigger input T of store flip-flop 88 is coupled a respective one of f_c signals from patch metwork 58 (designated f_{cx} herein).

The "1" output effstore flip-flop 88 is applied to one input of AND gate 98 with the other input being cou-